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by

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1.0 Introduction

This research was conducted in order to investigate and realize the monolithic integration of an InGaAsP/InP surface emitting LED Double Heterojunction Light Emitting Diode (DH) with an InGaAs/InP Heterojunction Bipolar Transistor (HBT) driving circuit. This report will describe the entire process of the research: design, growth, fabrication, characterization, and result analysis. The highlighted features of the system are its monolithic integration, surface emitting optical device design (LED in this case), and lateral, rather than a vertical, coupling of the LED and the HBT. The InGaAsP quaternary active layer of the LED is designed to operate at $\lambda = 1.55 \mu\text{m}$, which coincides with the lowest dispersion wavelength of silica optical fibers. Such an integrated structure is a prototype of an LED optical transmitter, which can be widely used in telecommunication and control applications.

1.1 OEIC Overview

The integration of InP-based double heterojunction surface-emitting light emitting diodes (DH SLED's) and heterojunction bipolar transistors (HBT's) on a single chip is a special application of the concept of optoelectronic integrated circuits (OEIC's), a concept was first proposed by Somekh and Yariv in 1972.[1] The fundamental idea of OEIC's is to monolithically integrate photonic devices and electronic devices with a single chip. The photonic devices include laser diodes (LD's), light emitting diodes (LED's), and photo-detectors (PD's), while the electronic devices are mainly FET's or HBT's. Two main material systems, GaAs and InP, are used today for OEIC's.

In competition with hybrid circuits, circuits in which discrete photonic devices and electronic circuits are assembled through wire bonding, OEIC's have inherent potential advantages of reduced size, high speed, low production cost, reliability, and ruggedness. Similar attributes of silicon IC's have brought the information revolution to our society with enormous commercial success.

The most important system applications of OEIC's are: 1—Telecommunications: It has been envisioned that a future service will become available that connects every house with a single optical fiber, capable of providing a single pathway for telephone, videophone, wide-band video, high-quality audio, and HDTV. Low-cost, compact, and reliable OEIC components are preconditions for such a system.; 2—Computing systems: The use of optical fiber for high-speed and high-volume data transfers between computers and between processors, or even optical computing with photonic logic and memory devices and circuits, have been demonstrated in a number of laboratories; 3—Military applications: The light weight of optical fibers, and the high speed potential for GHz range applications, and the expected higher reliability of OEIC's, are particularly suitable for military systems.[2]

Initial OEIC investigations concentrated on GaAs and lattice-matched AlGaAs alloys due to the relatively mature material and device technology for GaAs-based materials. In recent years, more effort has been applied to the research of long-wavelength InP-based materials ($\lambda = 1.1\text{--}1.6 \mu\text{m}$) because they match the low-loss and low-dispersion windows of silica fibers at wavelengths near $1.30 \mu\text{m}$ and $1.55 \mu\text{m}$ (hence desirable for long-distance optical communication) and the high-speed and large current drive advantages of InGaAs/InP HBT's. Considerable work has been done on InP-based OEIC receivers using p-i-n photodiodes with amplifiers comprised of MODFET's, HEMT's, or HBT's. Relatively little work has been done on OEIC transmitters of monolithically integrated LD's or LED's with HBT's or HPT's. To the best of our knowledge, there has been no report on monolithic integration of InP-based surface emitting LED and HBT drive circuitry.

1.2 Motivation for the Research

Although the recent development of laser sources has dominated OEIC research and applications, LED's represent an important complement to the LD's as alternative light sources. In the communication applications of moderate data rates and local-area networks (LAN's) or similar

short-haul networks, LED sources may be more desirable than LD sources in terms of cost efficiency, sensitivity to temperature, aging effects, and simplicity of operation. For example, AT&T has already installed an InGaAsP/InP SLED-based digital subscriber loop carrier system which can operate in nonrepeated ranges of up to 20 kilometers.[3] The choice of LED's for the light sources is due to special considerations of reliability and ruggedness, since the working environment is not temperature and humidity controlled, resulting in a great preference for LED's compared to LD's.

The high power handling ability and wide bandwidth of InGaAs HBT's make them very attractive for OEIC transmitter applications. The two predominant kinds of HBT's based on materials lattice matched to InP are: $\text{In}_{0.53}\text{Ga}_{0.47}\text{As/InP}$ HBT's and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As/In}_{0.52}\text{Al}_{0.48}\text{As}$ HBT's. The high electron mobility and velocity in the smaller bandgap base material InGaAs, together with the very thin epitaxial base width, lead to the excellent high frequency characteristics of the HBT's. Chen, et al. reported cutoff frequencies as high as 244 GHz.[4] The emitter/base heterojunction design with a wider bandgap emitter allows the HBT's to have very high current gain even at low voltage levels. The advantage of InGaAs/InP HBT's is that the valence band discontinuity is larger for InGaAs-InP than it is for the GaAs-based HBT's. Therefore, larger current gains are expected, because the common-emitter current gain is exponentially proportional to ΔE_v . Very high gain InGaAs/InP HBT's have been reported by Kyono, et al. at The University of Texas at Austin, with $\beta \sim 24,000$ and $h_{fe} \sim 49,000$. [5]

The work accomplished in this project can be readily applied to other optoelectronic integration problems. All the materials growth related research, the designs for devices, the device processing techniques, the layout masks and processing equipment, and the characterization techniques of this project can be directly transferred to the integration of InP-based vertical cavity surface emitting lasers (VCSEL's) and HBT's. The experience from this research will be very valuable for the VCSEL/HBT OEIC's, such as, the optical coupling effect expected between the LED (or LD) and the InGaAs HBT base, component isolation and connection, as well as the trade-off balance between optimizing photonic and electronic devices.

1.3 Challenges of Research Program

Despite the great promises of OEIC technology, it is mainly still at the laboratory research and development stage. The main challenges for further development and production are:

1.3.1 Material quality:

The nature of OEIC's requires multiple epitaxial growth of different layers, therefore defects and lattice mismatch associated with the heterointerfaces are severe problems. Moreover, the different optimization requirement for optical and electronic components may hinder the overall performance.

1.3.2 Structure compatibility:

Different sets of epitaxial layers for photonic and electronic devices are grown on a single substrate. To process and connect these components, the device structures and design layouts must be carefully carried out.

1.3.3 Process optimization:

Very high yield in production is the key factor that contributes to the low cost of OEIC's compared with hybrid circuits. In order to make Ohmic contacts to the devices and to isolate devices and components of an OEIC, mesa structures are normally employed. This results in a significant nonplanarity that may cause some areas to be out of focus during lithography and the metal interconnections may be forced to conform to relatively large step edges which will cause reliability and yield problems. Improved etchants with good selectivity and precise etch rates must be chosen for the device fabrication.

1.4 Program Overview

In this research program, preliminary investigations were carried out to explore and address the above issues. The work covered the complete cycle from initial device specification, device

design, epitaxial growth, and the processing of final prototype devices to evaluate performance. In the initial phase of this program, the InGaAsP materials required for these devices were grown and optimized conditions were used to grow specific device structures. Next, epitaxial films were processed into discrete devices to evaluate device performance. These discrete InGaAs/InP HBT's and InGaAsP/InP DH SLED's were studied in terms of device design, processing, testing, and optimizing. The relations between device electrical and optical performance and the epi-layer structure and device geometry were studied. Finally, circuit design using SPICE and mask design using AutoCAD tools were completed with consideration of the discrete device performance. Several drive circuits with different HBT sizes are incorporated onto the same set of masks for optimization.

2.0 Device Design Considerations

Individual device design is the foundation of electronic circuit performance. For the integrated optoelectronic transmitter (OEIT), the design of both electrical and optical devices should be studied. It is not the intention of this research program to achieve "top-gun" HBT's and LED's, but to correlate the device design with its performance, so that both HBT's and LED's can be engineered to meet system requirements.

The main issues for designing HBT's are the current drive capability (current gain, breakdown, etc.) and high-speed performance. The energy band discontinuities at emitter/base junction allow very high current gain without requiring the lowering of the base doping level, unlike the silicon bipolar transistor where low base doping is necessary for high current gain. This is a great advantage for the high-frequency performance where base resistance is the main obstacle to improve the cut-off frequency. Also, as shown in Table I,[6,7] the higher electron mobility of InP-based materials compared to Si and GaAs is an important advantage for InP-based HBT's high-speed performance.

The main issues for LED's are power output, efficiency, and modulation speed. The nature of spontaneous radiative recombination of an LED makes it inherently lower in power efficiency and modulation speed than lasers. Simplicity and reliability are the merits of LED's over laser diodes. Improving efficiency and speed are the main tasks for LED design.

Table I. Comparison of Material Properties of GaAs and InGaAs

Property	GaAs	InGaAs
energy gap, E_g	1.42 eV	0.75 eV
energy separation, $\Delta E(\Gamma-L)$	0.33 eV	0.55 eV
energy separation, $\Delta E(\Gamma-X)$	0.5 eV	1.15 eV
electron mobility, μ_e	8,000 $\text{cm}^2/\text{V-s}$	13,000 $\text{cm}^2/\text{V-s}$
electron effective mass, m^*/m	0.067	0.051
peak electron velocity, v_{peak}	2×10^7 cm/s	2.7×10^7 cm/s

2.2 InGaAs/InP HBT Design Considerations

The HBT is one of the most important applications of heterojunction design. Based on highly developed epitaxial technology, such as molecular-beam epitaxy (MBE) and MOCVD, bandgap engineering has opened a wide range of design options for device engineers. This freedom has been creatively applied to the design of a wide variety of devices such as: DH lasers and LED's, quantum-well devices, microwave devices, HBT's, and HEMT's, to name a few.

The innovative idea of employing different energy bandgap materials in a bipolar transistor was first proposed by Shockley in his patent filed in 1948.[8] The concept and the principles of heterojunction bipolar transistor were later discussed in detail by Kroemer.[9] The main advantage of a wider bandgap emitter is that both higher current gain and lower base resistance, which is essential for high-power and high-speed applications, can be achieved simultaneously.

2.2.1 Comparison of AlGaAs/GaAs and InGaAs/InP HBT's

The first material system which yielded promising HBT's was the AlGaAs/GaAs system. Recently the InGaAs/InP system has eclipsed the AlGaAs/GaAs system because of a number of significant advantages:

1. The relatively larger valence band discontinuity (0.37 eV) for InGaAs compared to $\text{Al}_x\text{Ga}_{1-x}\text{As}$ (0.20 eV for $x=0.40$). Such large discontinuities are desirable for achieving high gain HBT's with an abrupt emitter/base heterojunction;
2. Higher electron mobility in InGaAs ($\sim 13,000 \text{ cm}^2/\text{V-s}$), compared with GaAs ($\sim 8,000 \text{ cm}^2/\text{V-s}$) and Si ($\sim 1,350 \text{ cm}^2/\text{V-s}$) for low doping levels. This results in lower base series resistance and higher f_T 's are then expected.[6]
3. A larger separation of the Γ -valley from the indirect-gap satellite valleys in InGaAs than in GaAs, so that the transient electron velocity overshoot is greater in the former.
4. A smaller surface recombination velocity (10^3 cm/s) for InGaAs than that for GaAs (10^6 cm/s), which leads to smaller base recombination current and hence improves the base transport factor.[6]
5. Etchants with very good selectivity are available for the system so that very simple self-aligned device processing procedures can be employed.
6. The technological attraction of monolithic integration with InP-based photonic devices which could be operated at the wavelengths of 1.33 and $1.55 \mu\text{m}$ at which the silica fiber has lowest dispersion.[10]

2.2.2 Problems Associated With InGaAs/InP HBT's

Some challenges with InP-based systems are: (1) The diffusion of Zn is much faster in InP than in AlGaAs, therefore a lot of effort should be committed to achieving precise doping profile control; (2) The relatively small bandgap of InGaAs makes the base/collector homojunction susceptible to breakdown, hence limiting the power handling ability of the transistor. Several successful treatments have been employed to solve these problems, such as inserting an undoped spacer layer between the n-InP and p-InGaAs to prevent the misalignment of the electrical junction and the heterointerface, and using a very lightly doped collector or double-heterostructure to increase the breakdown voltage.

The heterogeneous emitter/base design is the most critical part of the HBT. The transport of electrons and holes across the heterojunction is directly related to the performance of the HBT, especially the common emitter current gain, β , (through the emitter injection efficiency— γ). For most contemporary HBT's, the base width is very small (typically $\sim 80 \text{ nm}$), so that the recombination in the base bulk is very small, hence near unity base transport factor α_T is expected.

3.0 Materials Growth

The InP based OEIT epitaxial layers were grown by low-pressure metalorganic chemical vapor deposition (MOCVD). The reactor is an EMCORE Model GS3200 UTM MOCVD system installed in the Microelectronics Research Center of The University of Texas at Austin. The system has a load-locked stainless-steel growth chamber that operates at a pressure of 60 Torr. The 5-inch diameter molybdenum wafer carrier is resistively heated and typically rotated at $\sim 1175 \text{ rpm}$ during the crystal growth. The reactant sources are accurately controlled with pressure balancing and temperature control and enter the reaction chamber through a pressure-balanced fast-switching injection manifold. Growth temperatures for InP and its alloys are $\sim 600\text{--}625^\circ\text{C}$. The sources for column III elements are: trimethylindium (TMIn), triethylgallium (TMGa), and trimethylaluminum (TMAI) from Air Products/Epichem. The column V sources are 100% arsine (AsH_3) and phosphine (PH_3). Doping sources are diethylzinc (DEZn) for p-type material and

tetraethyltin (TESn) for n-type material. Purified H_2 is used as carrier gas for all the precursor gases.

3.1 Lattice-Matching and X-ray Characterization

InGaAs is lattice-matched to InP at an alloy composition of $In_{0.53}Ga_{0.47}As$. After growth, the composition of an epilayer can be determined by performing an X-ray rocking curve scan. Figure 1 shows a typical rocking curve of an InGaAs single layer grown on InP. By noting the separation of the epilayer diffraction peak from the corresponding substrate peak, one can determine the composition of the film by assuming that the change in composition is a linear function of the change in lattice parameter of the film.[11] The InGaAs epilayer is grown such that it is lattice-matched at the growth temperature of $T_g \sim 625^\circ C$ so it is slightly compressively strained at room temperature.

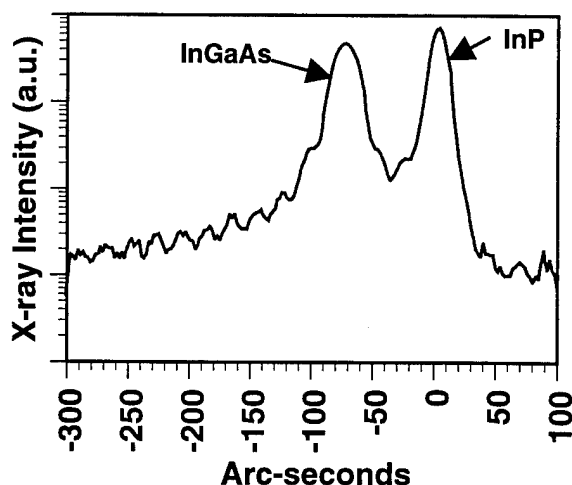


Figure 1: A typical x-ray rocking curve for an InGaAs layer on InP substrate.

More information about the crystallinity and the layer thicknesses and the composition can be found by performing x-ray simulation. Figure 2 shows that there is good agreement between

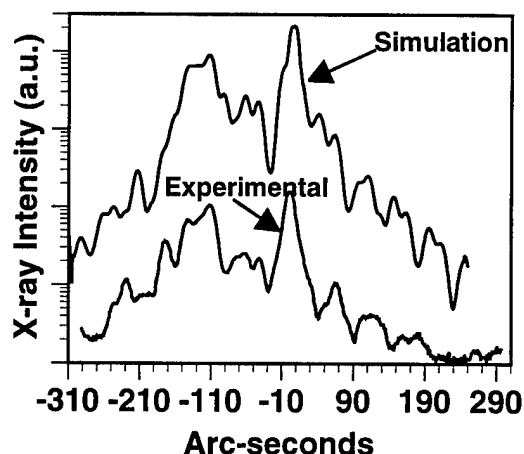


Figure 2: Experimental and simulated rocking curves for a HBT structure

the experimental and the simulated rocking curves for the HBT structure under study. The details of the diffraction simulation are very sensitive to strain at interfaces and the simulation shown in the above figure was done assuming abrupt heterojunctions and uniform compositions. Thus x-

ray rocking curve characterization can be a very effective tool in determining the structural quality of the crystal and abruptness of interfaces.

3.2 Doping Calibration

High-performance device structures in the InP-InGaAs materials system, such as HBT's, commonly require that highly doped, high-conductivity InP and InGaAs films be grown to lower the series resistance of the device and to make good non-alloyed Ohmic contacts. High doping concentrations of over $\sim 1 \times 10^{19} \text{ cm}^{-3}$ can be achieved for n- and p-type doping with the TESn and DEZn precursors, respectively.[12] This ability to heavily dope is critical to reduce the base resistance while keeping the base width small and thus achieving good high-frequency performance and a decent DC current gain, which provides the most fundamental performance advantage of HBT's over Si-based bipolar transistors. Doping concentrations ranging from $1 \times 10^{16} \text{ cm}^{-3}$ to over $1 \times 10^{19} \text{ cm}^{-3}$ for both n-type and p-type doping for layers grown at $T_g \sim 625^\circ\text{C}$. The low doping is possible because of a dopant dilution scheme used for the dopant lines in the MOCVD reactor. The carrier concentration in InGaAs vs. the vapor-phase mole fraction of TESn and DEZn are shown in Figure 3. Zn incorporation in InGaAs and InP is primarily substitutional below $1 \times 10^{19} \text{ cm}^{-3}$ but above this concentration the incorporation via interstitials increases leading to increased diffusion via an interstitial mechanism. This becomes important for preserving the integrity of the base/emitter heterojunction for HBT's with narrow base designs and high dopings. The variation in n-type carrier concentration vs. TESn mole fraction for InP is shown in Figure 4.

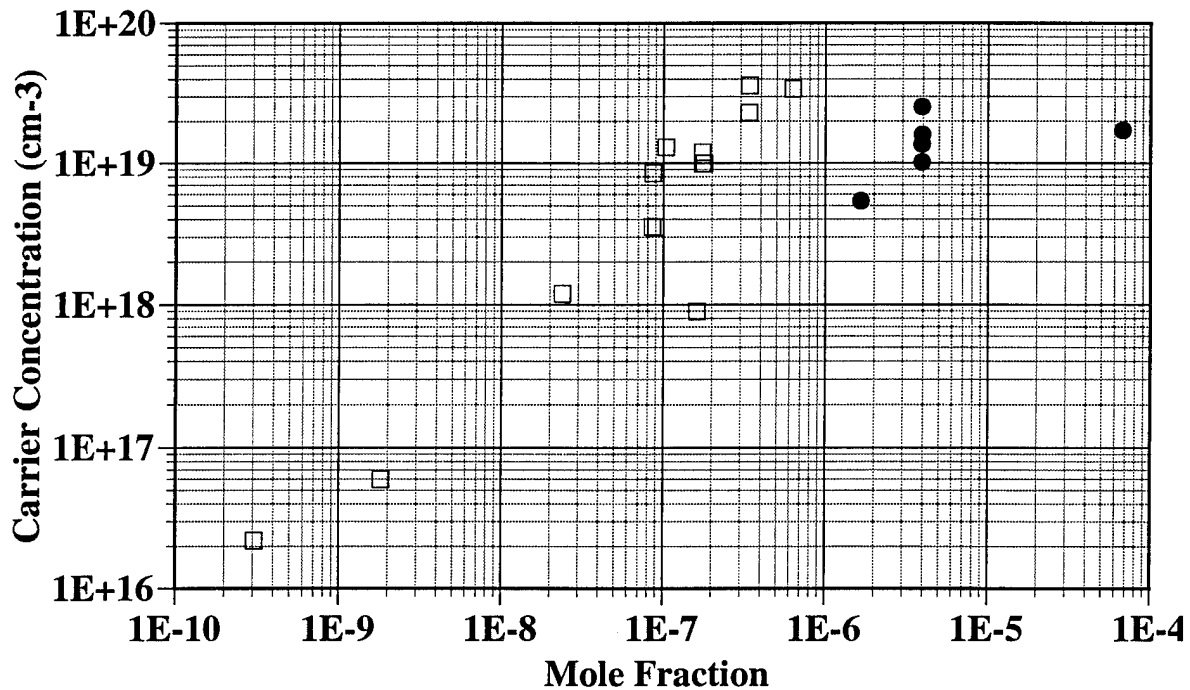


Figure 3: Carrier concentration vs. mole fraction of TESn and DEZn for InGaAs. The open squares are for Sn-doped InGaAs and the solid circles are for Zn-doped InGaAs.

As mentioned earlier, controlling Zn diffusion in InP and InGaAs has been a challenge to achieving accurate and sharp doping profiles at the emitter/base heterojunction and requires precise calibration of the growth conditions. A typical doping profile of the carrier concentration vs. thickness through the various layers of a typical HBT is shown in Figure 5. This profile was obtained using a electrochemical C-V etching method. The structure shown has a relatively low InGaAs base doping of $p \sim 4 \times 10^{18} \text{ cm}^{-3}$. A SIMS profile for the same HBT wafer is shown in Figure 6. The peak Zn concentration is the same indicating full activation of the Zn dopant. The

sharp turn-on and turn-off of the Zn and Sn dopant species implies excellent control of the doping level and profiles.

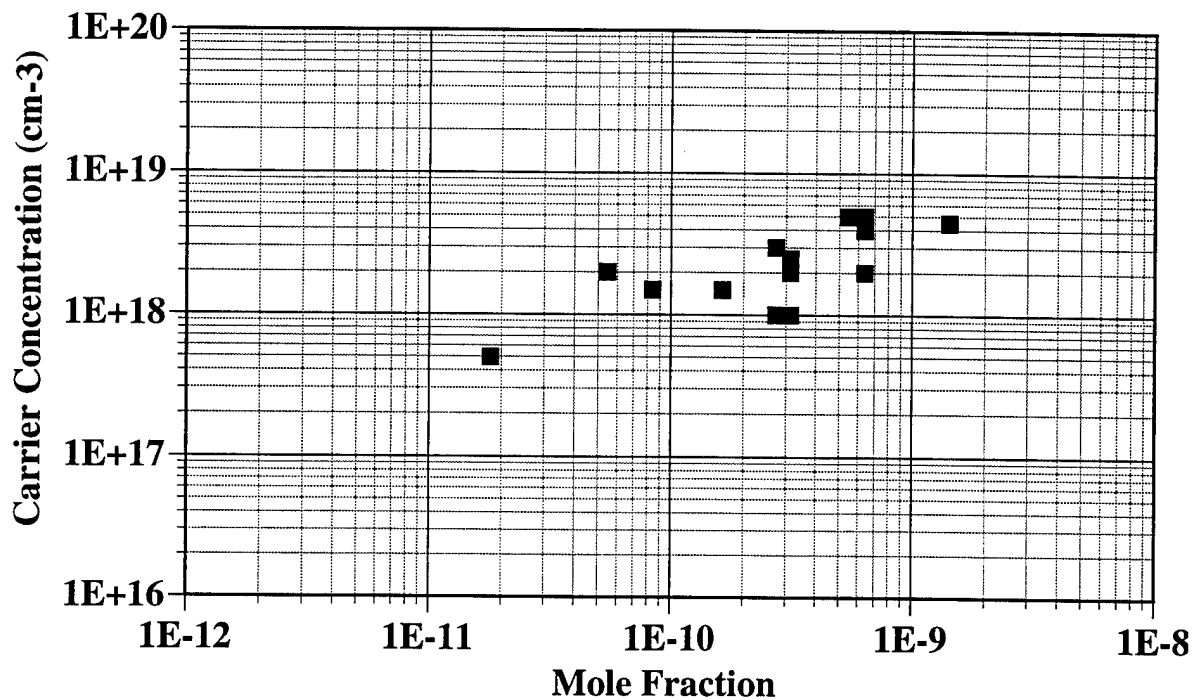


Figure 4: Carrier concentration vs. mole fraction of TESn for InP

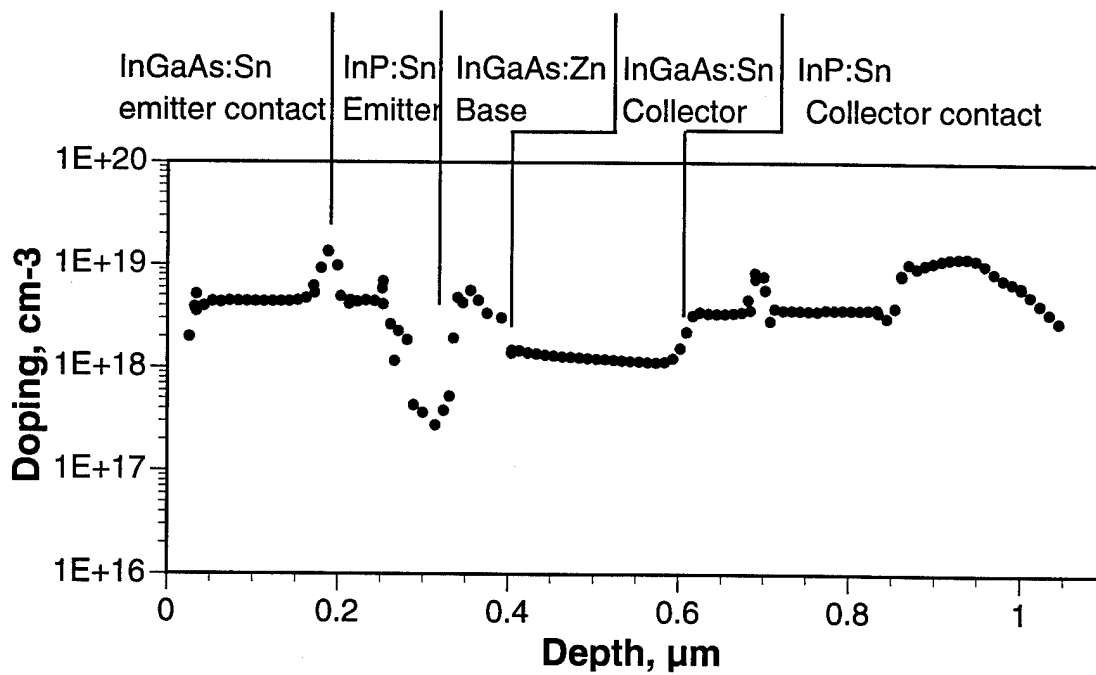


Figure 5: Electrochemical C-V curve showing the doping profile in a HBT structure with low base doping

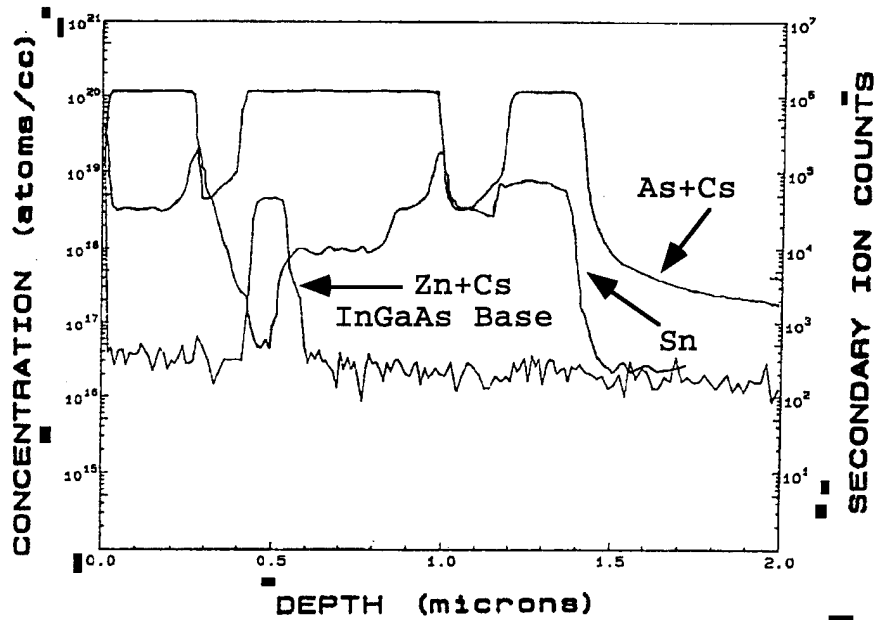


Figure 6: SIMS plot for the HBT structure with low base doping

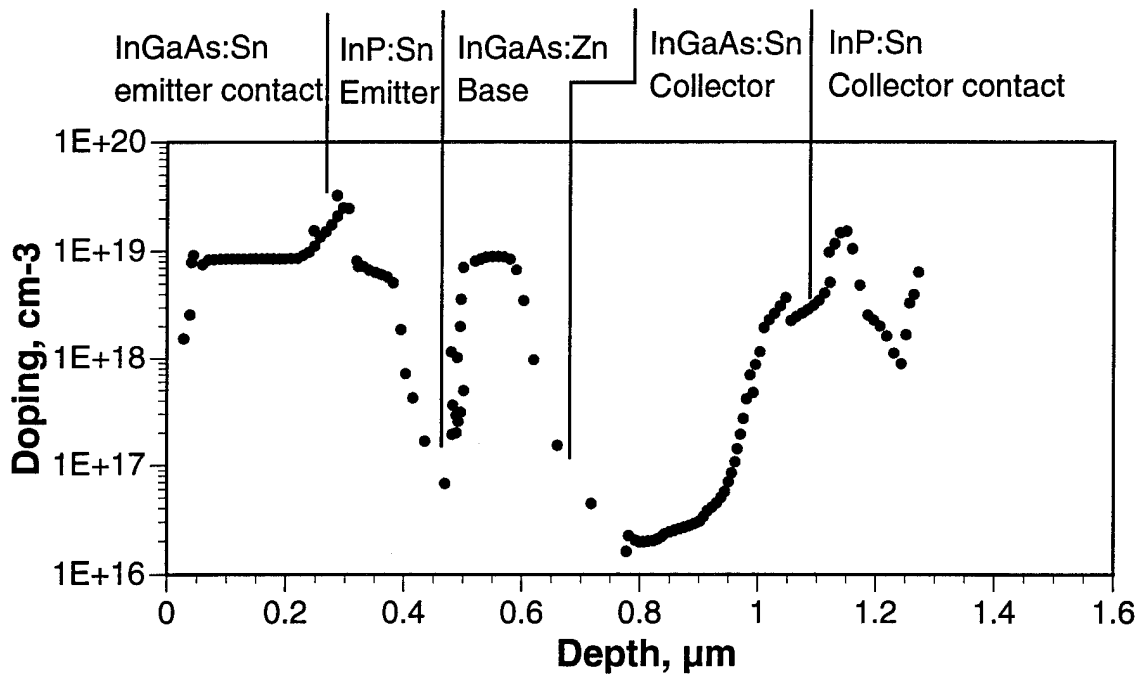


Figure 7: Electrochemical C-V curve showing the doping profile in a HBT structure with high base doping concentration.

4.0 HBT Device Processing and Testing

Extensive research on processing and testing of InGaAs/InP HBT's has been conducted in this program. A complete and mature processing procedure has been established, and successful device structures have been consistently realized.

4.1 Device Processing

The device processing mainly uses the following three techniques: lithography, selective etch, and metallization. A self-aligned process is employed to construct emitter and base mesas, which eliminates several steps of lithography and etching. The emitter, collector, and high frequency device contact pads are fabricated by efficient lift-off processes. Selectivity and etch rate of several etchants have been studied and employed in the processing. A new lift-off protocol, which needs shorter processing time and makes the metal lift-off more easily and completely, has been developed and applied in the processing.

The fabrication procedure can be briefly described as follows: The emitter patterns are first defined and then the mesa structures are formed by selective etching, which is followed by a metallization. The metal on the emitter mesas are removed by lift-off, and then the base patterns are defined and the excess metal is etched off. With the metal patterns as masks, the base mesas are formed by selective etch. Finally, the emitter and collector contacts are defined by the photoresist windows, and then the contact pads are constructed by following the metallization and lift-off. The complete processing run sheet is attached in Appendix D. The schematic diagram of the cross section of the HBT's at this stage is shown in Figure 8.

For the small high-speed HBT's and interconnections between devices, a layer of polyimide is deposited on the surface of the chip as described above. After the contact windows are opened in the polyimide, metal connection and pads patterns are defined. The metal evaporation and lift-off are performed afterwards, which completes the whole device processing. The high frequency characterization was conducted on an HP 8510B Network Analyzer. The s -parameters were measured and then the cutoff frequency, f_T , and the maximum oscillation frequency, f_{max} , was derived from it.

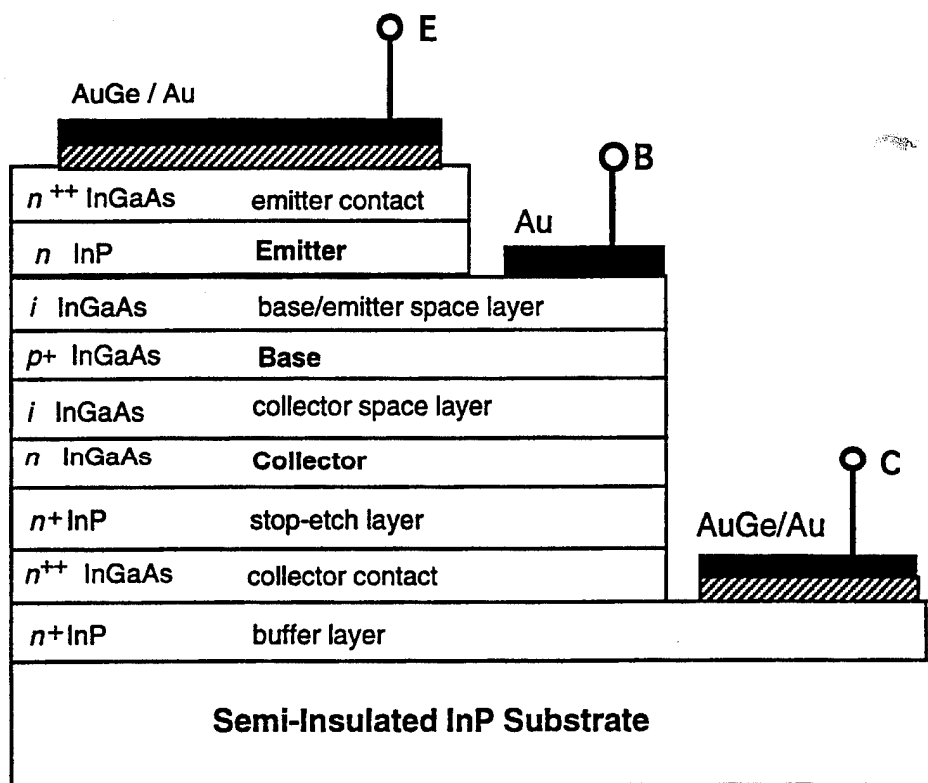


Figure 8: The cross section diagram of the HBT device structure.

4.2 HBT Device Testing

Steady-state characterization of the HBT's was carried out using an HP4145B Transistor Parameter Analyzer. Initially the measurements were conducted in a probe station designed for low-frequency characterization with needle-type probes, which are recommended for frequencies under 500 MHz. Strong oscillation constantly occurred during the testing voltage ramp, thus making the extracted data invalid. The oscillation was removed when the measurement was done on another probe station made by Wentworth Labs. For high frequency characterization, three-pin microwave probes by Design Techniques were used.

Experimental Gummel plot results were obtained from three sets of InGaAs/InP HBT's, HBT wafers #1, #2, and #3. The films were grown by MOCVD with base widths 80 nm, 100 nm, and 80 nm, respectively. Device parameters are extracted individually from the Gummel plots using a simple program written by one of the graduate students working on this program. Initial optimization was carried out by a library subroutine UNCMIN using a quasi-Newton algorithm.

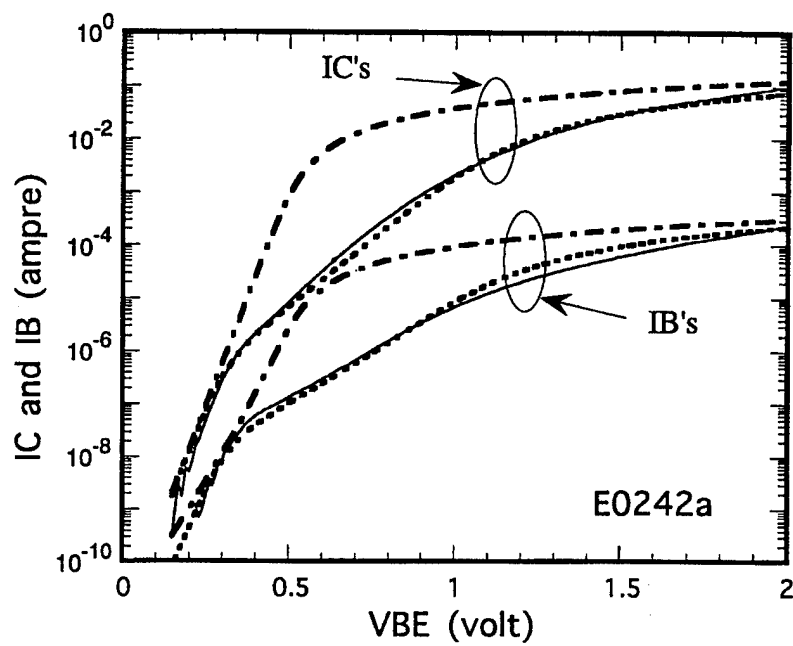
Numerical simulation of Gummel plots was conducted using the modified model. The results are shown in Figure 9, with experimental data and SPICE simulation results for comparison. The lack of constant current gains in the low bias region is attributed to the large dominant recombination current in the SCR of base/emitter junction.

It is observed in experimental Gummel plots that in the medium-bias region, the logarithm of the collector current depends almost linearly on V_{BE} , but with different ideality factors and saturation currents than is observed in the ideal (low-bias) region. Such changes cannot be simply explained by high-level injection effects, as it is usually treated. For HBT's, after the bending down of I_C as V_{BE} increases, the β does not decrease as expected in high-level injection for similarly structured thin-base homojunction bipolar transistors, where the high-level injection occurs when the free-electron concentration, n_o , is comparable to the base doping concentration, N_a .

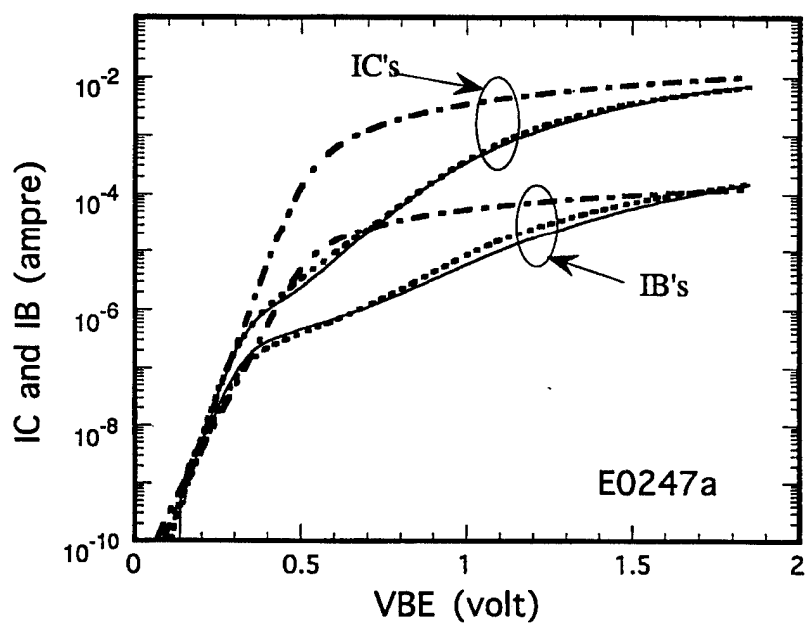
The emitter current, I_C , at the bending region is about 10^{-4} A and the emitter dimension is about $50 \mu\text{m} \times 50 \mu\text{m}$. Therefore the equivalent injected electron concentration in the base is $\sim 10^{12} \text{ cm}^{-3}$, which is much less than the p-type base doping level of $1.2 \times 10^{18} \text{ cm}^{-3}$. Numerically, the SPICE BJT model cannot fit the medium-bias range, where λ factors are greater than or close to 2, while here the factor λ would be fixed at 1. Therefore, for HBT's with such heavily doped base regions, the high-level injection effect should not be the dominant mechanism responsible for the I_C bending in the high bias region, but rather, we expect that the emitter resistance plays a more important role than it does in the BJT counterparts.

The fact that the λ 's are larger than 1, indicates that the drift effect is predominant when the HBT transport reaches the base-transport-limited regime at medium bias level. For the three sets of InGaAs/InP a-HBT's, the parameter λ is smaller for larger base width, W_B . This is expected from the proposed model, since the relative importance of the launch effect will decrease for larger W_B and in the extreme case of very long bases, diffusion current is expected to be responsible for the base transport characteristics.

In summary, a physical mechanism-based model to describe the abrupt junction HBT Gummel characteristics is established and evaluated numerically. The electron launching effect from the conduction band discontinuities is the primary cause for the abnormality at the medium biased operation regime. It has been shown that the high-level injection effect is not the reason for the current bending away from ideal curve, due to the high base doping level of the HBT's and the relatively low injection level. It has also been shown that the SPICE BJT model cannot be used to fit the Gummel plots over the whole device operation range, while the proposed modified model showed excellent agreement with the experimental results. Only two extra parameters are introduced in the model and their physical meanings are very clear. This model should be implemented very easily into a SPICE simulator to describe HBT dc behavior.

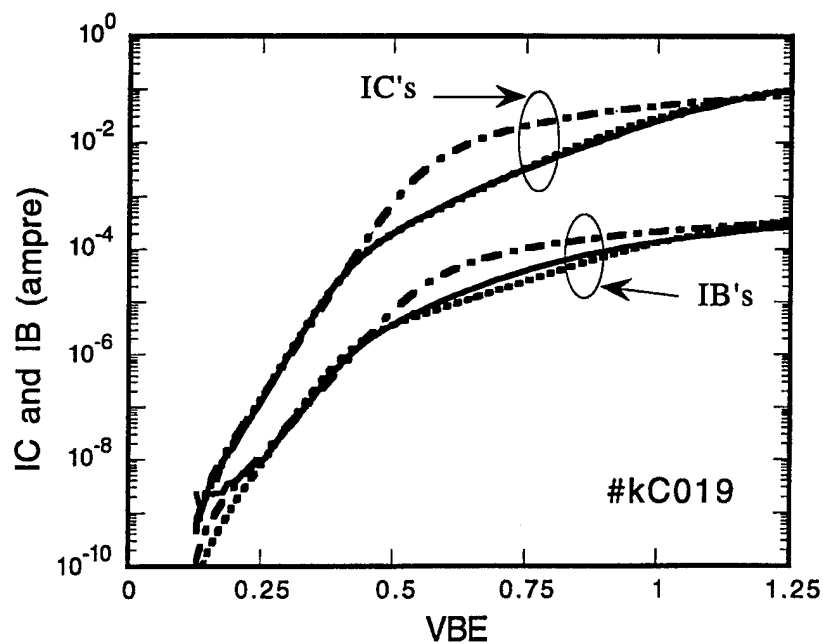


(a)

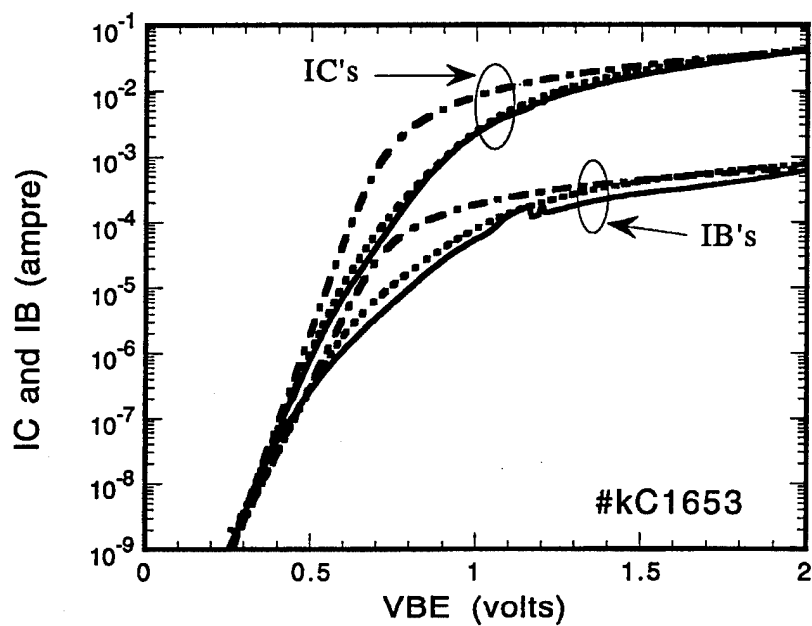


(b)

— experimental data; - - - PSpice; modified SPICE;



(c)



(d)

— experimental data; - - - PSpice; modified SPICE;

Figure 9: Four (4) Gummel plots with P-Spice simulated results for comparison.

5.0 LED Design and Processing

5.1 InGaAsP/InP LED Design Considerations

The light emission of LED's comes from the spontaneous radiative recombination of the excess carriers supplied by a forward-biased p-n junction composed of a semiconductor. For advanced heterostructure LED's, the carriers are normally confined in an active layer formed by a double heterostructure (DH), where the radiative recombination is designed to occur. Because stimulated emission is not intentionally implemented, the optical cavity and mirror facets are not required as in injection lasers. Therefore, LED's do not have an intrinsic threshold voltage and current as do laser diodes and may operate at much lower current densities. Because of the spontaneous nature of the emission, the light of LED's is incoherent and has wide spectral linewidth. The output light spectrum of an LED has a peak at the wavelength which typically corresponding to the active-layer bandgap energy, E_g . The peak of the emission spectrum will shift towards shorter wavelengths at high injection due to band-filling effects. The InP-based LED's normally have an InGaAsP quaternary active layer, which may emit near-infrared light in the wavelength range 0.9—1.6 μm .

In comparison with laser diodes, LED's have the following advantages that could be important in some applications:

1. Simple device structure (no cavity or mirrors), which leads to simple processing, thus high yield and low cost.
2. High reliability and long operating lifetime.
3. Low sensitivity to temperature; normally no complex temperature compensation circuitry is required.
4. Simple drive circuitry; because of low current densities and less temperature dependence, simple circuits without temperature compensation consideration can be used.
5. Linear dependence of output power on drive current, which makes operation easier and particularly suitable for analog applications.

LED's also have several disadvantages relative to injection lasers:

1. A relatively narrow modulation bandwidth, e.g., the normal modulation bandwidth of InP-based LED's is only several hundred MHz, compared to several tens of GHz for injection lasers.
2. Normally, a much smaller fraction of the emitted light is coupled into the optical fiber.
3. Harmonic distortion due to the relatively wider spectral linewidth.

Three considerations are most important in LED design. The first concern is to achieve the highest internal quantum efficiency, i.e., minimize nonradiative recombination and maximize the radiative recombination. The second consideration is to maximize the radiance which includes the maximum operating power and external quantum efficiency so that most of the emitted light will be coupled into the fiber. Finally, improving the high-frequency performance by maximizing the modulation bandwidth. In practical device and circuit design, trade-off's should be made between the above considerations in order to optimize the design to fit the overall circuit requirements.

Two types of LED structures have been developed and are categorized according to their geometry for light emission: surface-emitting (Burros type) and edge-emitting LED's. As the name suggests, an edge-emitting LED has an output window on the side of the active layer, while the surface-emitting LED has the light emitting window on the surface of the wafer/chip. The advantages of the surface-emitting LED are high radiance due to less internal absorption (shorter path in the active layer and the wider bandgap confinement layers are transparent to the emitting light), and the potential for monolithic integration with electronic devices.

5.2 LED Device Processing

The study of the discrete InGaAsP/InP surface emitting LED's was performed on the LED films. Successful LED structures have been fabricated and infrared light was observed from the LED's. The LED structure is similar to that designed for the integrated transmitter as shown in Figure 10. Here the metal contacts are the ring on the mesa and on the backside of the chip. The structure is chosen because of ease of fabrication and testing with the optical characterization equipment.

The device processing of the discrete LED's is compatible with that of HBT's and can be briefly described as follows. At first, the metal ring contact patterns are defined by lithography, next, metal is evaporated on the wafer surface, and finally, a lift-off process is used to remove the excess metal. Mesa structures are defined by lithography and constructed by selectively etching the quaternary contact layer, the InP confinement layers, and the quaternary active layer. Finally, the backside InP (substrate) is etched, while the device side is protected by white wax. Gold is deposited for the backside contact.

5.3 LED Device Results

The output light spectra for the fabricated LED's were measured with an HP 70951A Optical Spectrum Analyzer with a sensitivity range 0.6—1.7 μm . A 100 μm -diameter multimode graded-index fiber with a lensed end was mounted on a micro-manipulator and the lensed end was placed directly above the LED light emitting window. The other end of the fiber was coupled to the optical input port of the HP 70951. The dc electrical bias was provided by a Precision DC Source model 2020B which has an operating range of 0—20 V and 0—2 A. The measured output spectra of the LED's indicate that the peak wavelength is $\sim 1.542 \mu\text{m}$, which is very close to the targeted wavelength of 1.55 μm . It means that very accurate compositions of In, Ga, As, and P sources were achieved during the MOCVD crystal growth.

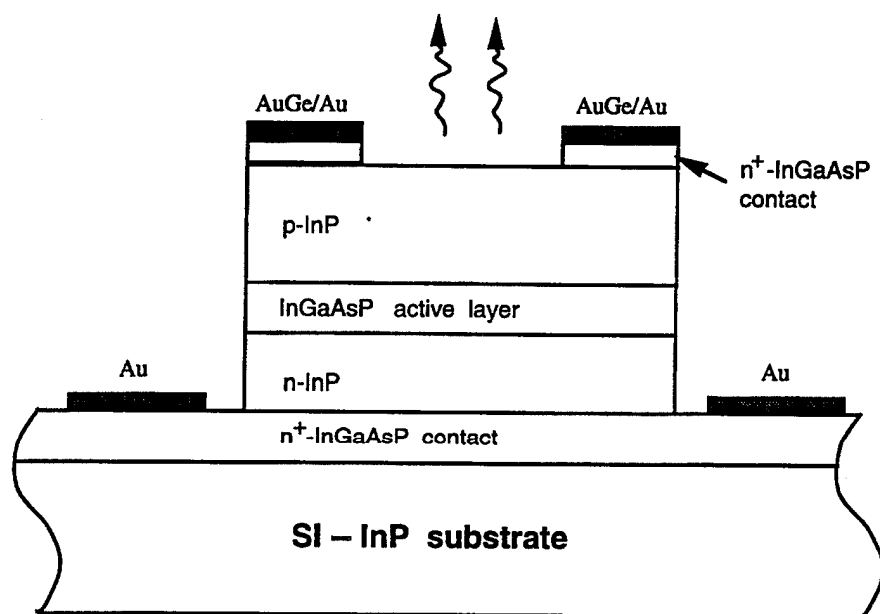


Figure 10: The LED device structure for the integrated transmitter.

6.0 Summary of Discrete Device Results and Discussion

As stated in the introductions, this research project was intended to confirm the feasibility of the monolithic integrated OEIT constructed by InP based HBT's and LED's. Careful design of the epitaxial layers and devices, successful crystal growth, and accurate device and circuit processing are prerequisites for a working OEIT.

Discrete devices (test HBT's and LED's built along with the OEIT) were characterized to confirm the successful achievement of the specified individual device performance. For the HBT's, steady-state (dc) measurement and analyses were conducted in terms of emitter/base and collector/base junction I-V characterization, transistor Gummel plot of I_C and I_B versus V_{BE} and curves of I_C vs. V_{CE} by stepping I_C . Scattering parameters were also measured and h_{21} was calculated and f_T and f_{max} were extracted. The performance of the fabricated HBT's were well within the designed range.

The steady-state characterization of the LED's in terms of current vs. voltage and current output vs. optical power were carried out. Typical LED performance was obtained. The spectral measurement of the emission revealed that the output light wavelength (1.54 μm) was very close to the designed wavelength—1.55 μm . Successful operation of the LED's was confirmed.

Working individual devices, HBT's and LED's, on the integrated structure are essential, but not sufficient, to have a working integrated OEIT. Interconnects and isolation with good characteristics are equally vital to achieve the fabrication of a successful integrated OEIT. The OEIT's with single HBT drivers were tested with emphasis on high-frequency modulation (bandwidth) characterization. Very good dc operation was obtained in terms of current gain and signal amplification. The moderate small-signal modulation speed achieved was in line with the designed structures compared to the reported similar discrete LED's. The low optical power resulted from the low LED external efficiency and coupling losses in the measurement system and strong oscillation was observed in the measurements. Discussions and suggestions for further improvement to have high performance integrated OEIT's are presented in the next section.

7.0 OEIT Testing and Results

7.1 OEIT System Performance

The dc electrical characterization of the integrated OEIT circuit was performed first to confirm its designed characteristics. Due to severe oscillation of the circuits when tested using simple needle probes, the microwave probes were used for both signal input bias and dc power supply inputs. Thus, the probe set up was similar to the testing equipment set-up for high frequency OEIT characterization.

The family of curves of the OEIT is shown in Figure 11. Here the LED acts as a load to the single HBT driver. Good amplification of the input dc signals was obtained. The PSpice simulation results are shown in Figure 11(c) for the small HBT/LED circuit, and these predictions had very good agreement with the experimental data as shown in Figure 11(a).

The high-frequency characterization of the OEIT requires three types of equipment: (1) variable-frequency electrical "drive" signal generation, (2) electrical dc biasing and dc power supply, and (3) optical signal extraction and processing. The testing equipment set up is schematically shown in Figure 12. The OEIT (DUT, device under test) was put on a platform, where the probes and optical fiber can reach the designated positions. The input signals were generated by a HP 3314A Function Generator which has frequency sweep up to 20 MHz. The input device was bias by a Precision DC Source. The small signals and dc bias were coupled into the input device through a bias-Tee. The p-type end of the LED was biased with another Precision DC Source. A high frequency photo diode was connected to a two-stage amplifier, Mini-Circuits ZFL-1000LN, with total amplification of 100 times. Then it is connected to an HP 8566B Spectrum Analyzer with frequency range of 100 Hz—22 GHz. The fiber was coupled to the photodiode through a lens. Due to severe broadcasting during the measurement, the photodiode and all bias-Tee's were shielded by aluminum foil. The high frequency characterization of the OEIT, the plot of bandwidth, is shown in Figure 13.

The very low signal-to-noise ratio observed here can be attributed to the low external efficiency of the LED's, fiber-to-LED coupling loss, and fiber-to-photodiode coupling loss. The way the bandwidth was measured with such a low S/N ratio was that the light between the lens and the photodiode was blocked by a piece of aluminum foil during the signal sweep. Thus the

background noise was composed of all system noise plus the broadcasting noise, e.g., the small peak around 1.2 MHz shown in Figure 13.

7.2 Discussion of Results

Acceptable dc performance for the OEIT's fabricated in this program has been obtained in terms of HBT current gain and LED output light wavelength, linearity of optical power vs. current. High frequency signal modulation was achieved with the OEIT. One of the most noticeable performance problems is the weak optical signals, i.e., low LED external efficiency and low coupling efficiencies in the measurement system. In this section, several important performance issues, LED efficiency, possible substitute of polyimide, and layout pads design, will be discussed and some suggestions for future improvement will be given.

The bandwidth is about 5.5 MHz at $I_C = 15$ mA which is smaller than a similar discrete LED (~20 MHz) reported by previous workers. This was expected because of larger parasitic capacitance associated with this integrated surface-emitting LED structure due to the larger active junction area and shorter contact distance. Further improvement possibilities will be discussed in the next section.

7.2.1 LED Performance:

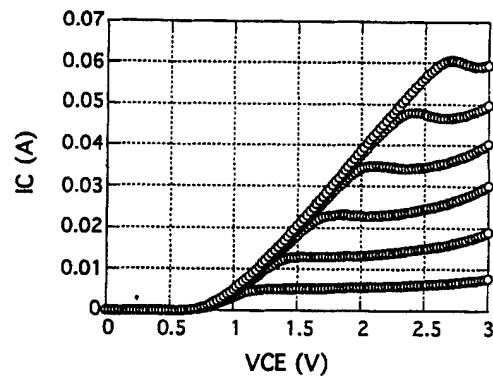
Two major structural problems are the main reasons causing the relatively low LED external quantum efficiency: (1) the large p-type contact area and/or area of the light-emitting region in the active layer, and (2) a flat light-emitting surface. In most discrete surface-emitting LED designs, the contact opposite to the light-emitting window is very small and positioned in the center, so that the current is confined in a relatively small area in the active layer. The light-emitting region, the part of the active layer with most of the current flowing through, is in the center of the light-emitting window and is fairly small in size. The LED's in this OEIT have p-type contact layers with the same size as the quaternary active layers. The top n-type contact ring makes most of the current flow through the edge of the LED mesa to the p-type metal contact. Therefore the light-emitting region will be a ring along the outer edge of the active layer. Obviously, most emitted light is blocked by the upper metal contact layer, and the part of the light reaching the window region is partially blocked by internal total reflection. Little light can be extracted from the light-emitting window in this structure. This is confirmed by the observation during OEIT measurement that more light can be extracted from the outer edge of the LED mesa than that from the center of the light-emitting window.

7.2.1.1 Improved Quantum Efficiency:

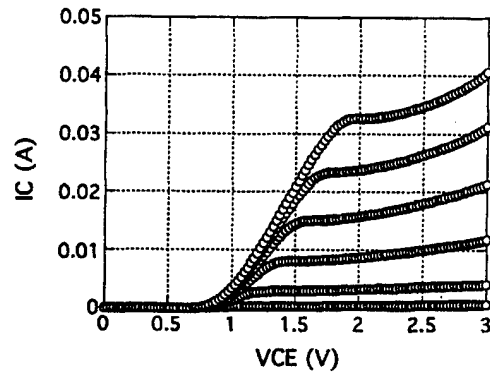
The problem of internal total reflection at the light-emitting window can be partly solved by making a spherically lensed window surface, which can be formed by applying ion-beam etching with a deformed photoresist layer as an etching mask. However, the effectiveness of the lensed window is somewhat overshadowed by the fact that the light-emitting region is not aligned to the center of the light-emitting window.

To make the p-type contact layer confined to a small area at the center of the LED mesa is no trivial task. The contact layer is buried under a whole deck of epilayers and no conventional processing techniques can reach the contact layer without affecting other epilayers. Selective crystal growth or multistep crystal growth could form a small area contact layer, by etching patterns on the contact layer and then growing other epilayers on top of it. But later pattern alignment during device/circuit processing will be prohibitively difficult.

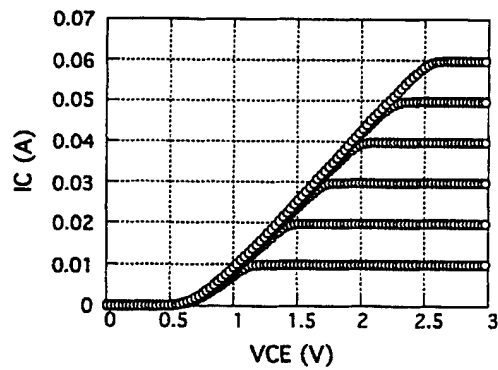
One possible way to form a smaller and centered active layer is to create excessive undercut of the active layer by over-etching the active layer during LED mesa formation. In this approach, smaller n^+ -type InGaAs contact layer area on top of the LED mesa compared to the n-type InP confinement layer is needed to prevent severe undercut of the contact layer. This process is completely compatible with current processing techniques and requires no new epilayers (just one extra mask level is needed). The thicker active layer, however, may be needed for better undercut result. Strong stirring during the etching, such as ultrasonic rinsing, might also be needed for deeper undercut.



(a)



(b)



(c)

Figure 11: Family of I-V curves for a fabricated OEIT: (a) small HBT driving a small LED, and (b) large HBT driving a large LED. Both figures have current steps of $I_B = 100 \mu\text{A}$. (c) P-Spice simulation of small HBT/LED OEIT, family of curves with $I_B = 100 \mu\text{A}$.

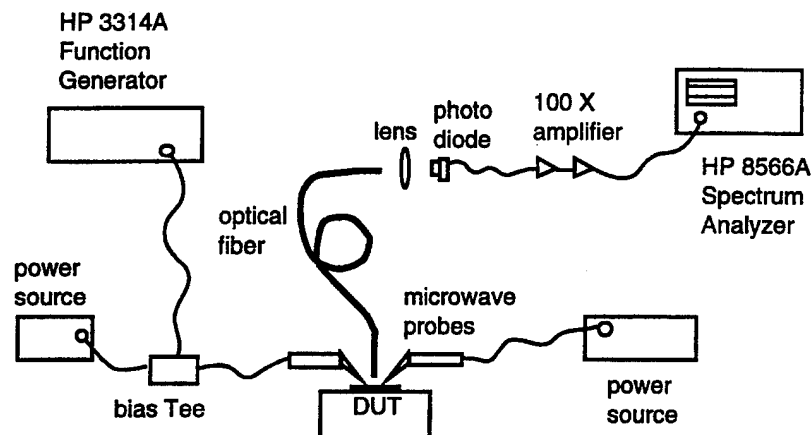


Figure 12: OEIT bandwidth measurement equipment set-up

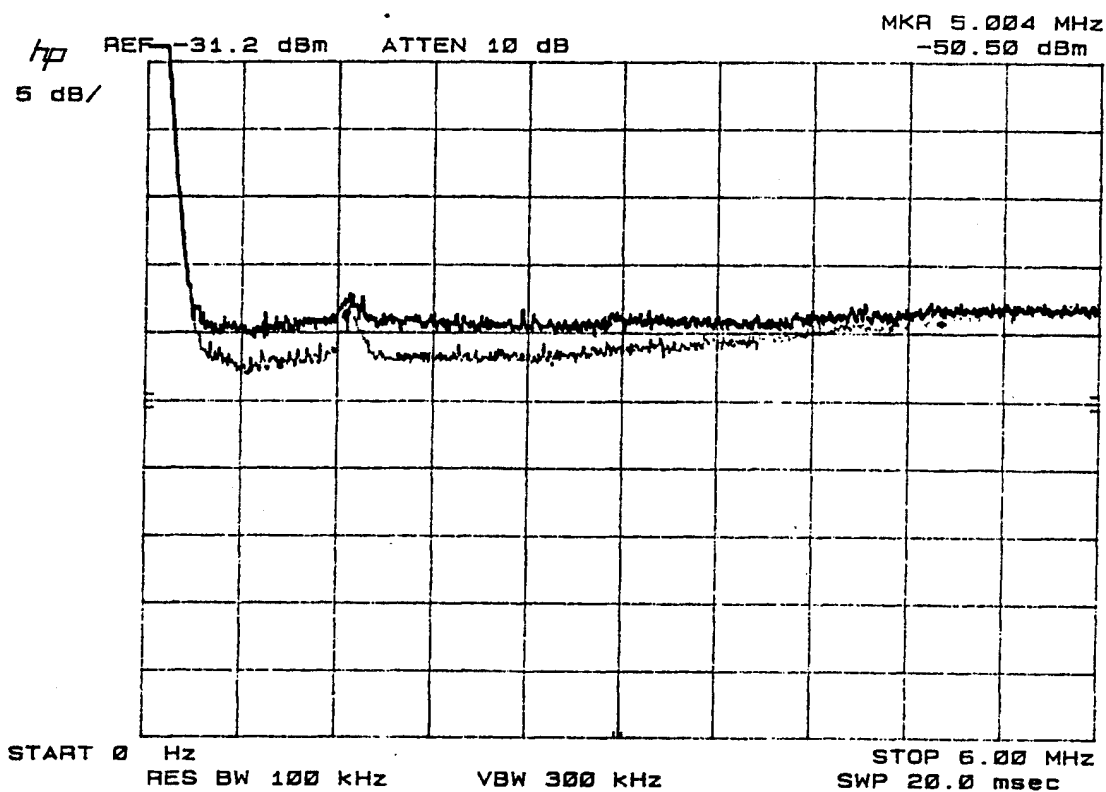


Figure 13: OEIT bandwidth plot. HP3314A signal amplitude = 0.1 V. Bias $I_B = 400 \mu\text{A}$ and $V_{CE} = 2.0 \text{ V}$, and $I_C = 15.3 \text{ mA}$. The dark line is signal and the light line is the background noise.

7.2.1.2 Improved Frequency Response:

The active layer was very lightly doped for improved optical power output. As a result, the LED modulation speed was inevitably sacrificed. The large junction area between the active and the p-type contact layers, together with relatively thin n-type confinement layer, will lead to larger parasitic capacitances, which further degrades the high-frequency performance of the LED's.

The proposed active layer undercutting will also improve the high-frequency performance by reducing the active area. The thickness of the epilayers is not recommended to be increased substantially, because prolonged crystal growth will cause severe dopant outdiffusion in the initial epilayers, as was observed for Zn out diffusion in the p-type LED contact layer, which will make the device performance unpredictable. With improved output optical power, different doping levels for the quaternary active layer should be investigated to increase the modulation speed without sacrificing too much of the optical power.

7.2.1.3 Improved Device Processing:

Some steps in the OEIT processing could be improved by employing alternate techniques. In this section, selective etching and polyimide isolation/via processing are discussed in terms of present problems and possible future improvements. The epilayer thickness limitation due to out-diffusion is also discussed.

Selective wet-etching process was used extensively in the OEIT processing to form various mesa structures. The advantage of this wet etching is its excellent selectivity between InGaAs and InP, which is essential for successful fabrication of OEIT's. However, one undesirable side effect associated with this wet etch is severe undercut, due to the isotropic nature of the wet etch. The base Au contact metal came off because of the underneath InGaAs base/collector layer undercut was often encountered and the HBT failure rate was high on these wafers (due to the shortened base/collector junction). Moreover, consistency between each etch is difficult to maintain. Therefore, selective, anisotropic, highly controllable dry etching techniques for InP-based materials are well worth being explored for future OEIT research.

Polyimide films have been widely used as isolation dielectrics and partial planarization in integrated circuit processing. In this OEIT, the polyimide films provided very good electrical isolation and topological planarization. However, the polyimide films are somewhat too soft for the purpose of supporting metal pads during probing. Many devices and circuits were ruined due to smashed probing pads, although extreme care had been taken in probing. It is difficult to land the three-pin microwave probes properly (fully contacted and yet not too hard) on the metal pads.

Another dielectric material often used for planarization and interlevel isolation in IC fabrication is spin-on glass (SOG). Similar to polyimide, SOG is applied in liquid form and spun on the wafer, then partially cured, patterned, and then fully cured. SOG materials are sioxanes or silicates mixed in alcohol-based solvents. Upon baking, the solvents are driven off and the remaining solid film exhibits properties similar to those of SiO₂. Therefore more solid mechanical strength is expected from SOG films than from polyimide films. Also SOG has good conformity as polyimide that can alleviate the high mesa and sharp edge problems associated with the OEIT. Therefore, SOG isolation layer is recommended for future InP-based OEIT's. However, potential problems associated with SOG should be addressed first, e.g., nonadhesion to various surfaces, cracking after cure for thick films, and poisoning of surfaces, the effect of outgasing of the SOG during the second metal evaporation, resulting in high contact resistance between two metals at the vias.

7.2.2 OEIT Design:

Several important features of the OEIT performance could be improved through design and processing changes. Some of these are discussed below.

7.2.2.1 Improvements for High-Current Drive:

The surface emitting LED's have inherent low external power efficiency. Therefore high current drive is desired to generate more optical power from the LED's. Several issues should be

considered as increasing the electrical drive. First, compatible HBT's are required for such large current drive. Larger geometries and high breakdown voltage epilayer design should be employed for the HBT's. Also, fairly thick Au interconnect layers are required to endure the large current. Burn down of the Au wires occurred once during the high current drive testing for the LED.

7.2.2.2 Improved Heat Sinking:

Another important issue is the heating problem due to such high power operation. The design of heatsinks is one of the approaches employed to address this problem in some hybrid circuits. An integral heatsink design for GaAs MMIC's, in particular, for the case of power GaAs FETs, the devices are thermally isolated by etching backside trenches, and the heatsink is formed by filling the well with gold by electroplating. Problems with this integral heatsink are that mechanical support for the chip will be difficult due to the trench isolation and hence the yield will be lower. Although the processing techniques involved here are fully compatible with the conventional MMIC processes, the infrared alignment system, which is not available in this laboratory, is required to align the backside heatsink patterns with the devices on the front side.

7.2.2.3 Optical Output Power Stabilization:

The function of a current stabilizer is to isolate the optical output power from the fluctuations of the device supply current and temperature. Output optical power temperature dependence stabilization should also be addressed in future OEIT research. Because the output power of an LED has an exponential dependence on temperature, temperature compensation of the output optical power is necessary especially in high power operation. This is especially true for monolithic integrated transmitters where heatsinks are extremely difficult to realize.

To compensate for the temperature effects, the drive current should be increased as the LED temperature rises to stabilize the optical power. Few studies have been reported on the temperature compensation of monolithic integrated transmitters, while most researchers have focused on the drive circuit bias stabilization.

7.2.2.4 High-Frequency Contact Pad Design:

Several improvements to the design of the contact to the OEIT can be proposed:

1. Employ microwave pads for all contacts, with all grounded pads connected.
2. The amplifiers (transistors) should be positioned very close to the ground bus to minimize common-ground inductance.
3. Cross-talk between probes—>might cause oscillation, so the pads should be spaced farther apart.
4. Less capacitive overlap of metal interconnects and underneath layers.

In OEIT characterization, to avoid oscillation, three-pin microwave probes were used for all contact pads. The microwave probes have a ground-signal-ground (GSG) configuration, i.e., the outer two pins are grounded. In probing some of the pads, the outer two pins were not grounded because the pads were initially designed for needle probes. By high-frequency layout design rules, all grounded pads should be connected and placed as near as possible for lower impedance at high frequencies. Therefore, additional grounding pads are needed for those probing locations.

The HBT's should be positioned very close to the ground bus in order to minimize common-ground inductance, which, in turn, will suppress crosstalk between probes. Wide common ground metallization will also help to reduce the inductance. Also the spacing between input and output should be as far as possible to avoid crosstalk between probes.

In future OEIT layout design, the overlap between metal interconnect lines and underneath conductive layers should be minimized to reduce parasitic capacitance. In this OEIT layout, a large ISO2 (LED p-type contact layer) was designed for easier alignment, which should be reduced in future redesign. Also, direct crossover of the metal lines should be avoided for the same reason.

8.0 Summary and Conclusions for OEIT Circuits

The goal of this work has been to demonstrate the feasibility of an InP-based monolithic integrated optoelectronic transmitter (OEIT), which is composed of InGaAs/InP single-junction HBT's and InGaAsP/InP double-heterojunction surface-emitting LED's. The design philosophy of the OEIT's was an integrated consideration of system, device, circuit, layout, processing, and crystal growth. The final characterization confirmed that working OEIT's have been fabricated with expected dc electrical performance, accurate LED output light wavelength, and high-frequency small-signal modulation response.

Individual discrete devices, HBT's and LED's, were first studied to provide basic information on epilayer quality and device performance. A novel LED structure was employed for the OEIT, because of the requirement that both contacts must be on the same side (device side) of the wafer.

Considerations on the system level were carried out in terms of the OEIT performance requirements, structure and performance compatibility of the devices, and processing flow design, which provided general guidelines for the following detailed design considerations. Simple circuit configurations were employed for the OEIT's because of the emphasis on the workability, not the ultra-high performance, of the OEIT's. More complex and high-performance circuits can always be implemented in the future research.

In the layout design, device sizes and structures were determined with the experience on the previous individual device researches, such as the 45-degree rotation of the HBT mesas from the [100] crystal planes. Some system issues were also taken into account, e.g., sparse placement of the devices to avoid local intensive heat generation, high-speed probe pad arrangement, and compatibility with the processing techniques available. Both light- and dark-field masks were used in the mask set. A special image-reversal process was employed to fabricate the light-field masks, while conventional positive photoresist was used for the dark-field masks.

Epitaxial growth of complicated InGaAsP-InP device structures was achieved using state-of-the-art MOCVD growth. Excellent crystal quality and epilayer thickness and doping level control were the foundation for achieving the working OEIT's. Good performance of the HBT's and LED's, especially low junction leakage and near unity of the ideality factors of the heterojunctions, confirmed good lattice match of the epitaxial films.

After the crystal growth was carried out, the films were processed in the device processing laboratories. The processing of the OEIT's was based on the combination of the processing procedures of the HBT's and LED's. Selective mesa etching, metal evaporation and lift-off, and photolithography were the core techniques involved in the OEIT processing. Steep vertical structures, i.e., very high mesas (up to 4 μm), created some difficulties in the final lift-off processes. Thick photoresist was applied and ultrasonic rinse was employed during the lift-off to completely remove the undesired metal layers. A removal of the thin base set-back layer before base Au metallization was added to the OEIT processing to ensure good Ohmic contacts by exposing heavily doped base layer to the Au. The final Au metallization was double-coated to increase the thickness of the pads for better probing damage resistance.

The dc characterization of the HBT's on the OEIT chip demonstrated good emitter/base and collector/base junction characteristics and agreed well with the predicted transistor performance in terms of current gain. Higher f_T 's than predicted by the SPICE model (up to 10.5 GHz) were obtained. The HBT mesa undercut which occurs during etching for contacts may be the cause of these better-than-expected results. The dc measurements of the tested LED's revealed excellent p-n junction diode current-voltage characteristics. The wavelength of the peak of the emitted light, measured at 1.54 μm , was very close to the designed wavelength of 1.55 μm . The dc characterization of the OEIT's indicated very good signal amplification. Small-signal modulation was achieved with bandwidths up to ~ 10 MHz.

The performance limitation of the OEIT's is the relatively low external quantum efficiency of the LED's. LED structural change recommendations are given in the above discussion. Also given are suggestions for improvements in OEIT device processing (e.g., using a polyimide

substitute), larger HBT's for larger current drive and associated heat dissipation, as well as improved power-stabilization solutions, and a common-grounded contact pad configuration to suppress the circuit oscillation for the devices under test. These recommendations and suggestions are well in line with the other primary goal of this work, namely that future development of OEIC's, especially OEIT's with vertical-cavity surface-emitting laser diodes (VCSEL's), may be derived from this research.

9.0 References

1. S. Somekh and A. Yariv. *Fiber Optic Communications*. In Proc. Conf. International Telemetry, pp 407-418, Los Angeles, 1972.
2. M. Dagenais, R. F. Leheny, H. Temkin, and P. Bhattacharya, J. Lightwave Technol. **8** 846 (1990).
3. P. P. Bohn, C. A Brackett, M. J. Buckler, T. N. Rao, and R. H. Saul. AT&T Bell Laboratories Tech. Jour. **63**, 2389 (1984).
4. Y. K. Chen, A. F. J. Levi, R. N. Nottenberg, P. H. Beton, and M. B. Panish, Appl. Phys. Lett. **55**, 1789 (1989).
5. C. S. Kyono, N. D. Gerrard, C. J. Pinzone, C. M. Maziar and R. D. Dupuis, Electron Lett. **27**,40 (1991).
6. P. M. Asbeck. Bipolar Transistors. In S. M. Sze, editor, *High-Speed Semiconductor Devices*, Chapter 6. (Wiley & Sons, New York) 1990.
7. R. N. Nottenberg, *Microelectronic Engineering*, **15**, 303-312 (1991).
8. W. Shockley, 1951. U.S. Patent 2 569 347.
9. H. Kroemer, *Proc. IRE* **45**, 1535 (1957).
10. J. M. Senior. *Optical Fiber Communications*. (Prentice-Hall, New York) 1985.
11. J. Hornstra and W. J. Bartels. J. of Crystal Growth **44**, 513-517 (1978).
12. C. J. Pinzone, N. D. Gerrard, R. D. Dupuis, N. T. Ha, and H. S. Luftman, J. Appl. Phys. **67**, (1990).

10.0 Appendix I: Native Oxide Research

10.1 Introduction

During the course of this research program on integrated optoelectronic transmitters, our work on high-performance III-V compound semiconductor devices was expanded to include research on III-V native oxides, an important new technology which could have broad application in the area of high-speed, low-power electronics as well as integrated optoelectronics. This technology was pioneered by Prof. N. Holonyak, Jr. at the University of Illinois at Urbana-Champaign (UIUC) in 1990 (sponsored by ARO). We have undertaken research in this area and investigated some of the fundamental process parameters for this technology, including the first measurements of the minority carrier lifetime in quantum wells with native-oxide regions. In addition, we have applied our results to the fabrication of vertical-cavity surface-emitting lasers, field-effect transistors, and also to light-emitting diodes. Much of the work in this area carried out by Dupuis' group has been performed in collaboration with Prof. Holonyak and Prof. Gregory E. Stillman and their groups at UIUC.

Several publications related to this research have acknowledged support from this ARO program. They are listed below in Appendix II as are the papers we have given at several conferences on this topic. In addition, we have recently submitted two related abstracts to be presented at conferences this year.

10.2 Summary of Native Oxide Results

Dupuis' group at UT-Austin has extensive experience in the native oxidation process in many of the InAlGaAsP alloy systems. For example, as mentioned briefly above, we have examined the luminescence behavior of MOCVD-grown InGaP/InAlP quantum-well (QW) heterostructures with oxidized InAlP cladding layers. This collaboration has led to the first demonstration of optically pumped room-temperature (300K) laser operation of VCSEL's employing native-oxide/semiconductor high-reflectivity DBR mirrors.¹ In other experiments, both photoluminescence (PL) and time-resolved photoluminescence (TRPL) characteristics of these samples have been characterized. These initial studies show significant improvements in PL and TRPL performance when increasing thicknesses of the top InAlP cladding are converted into native oxide layers.² In this ARO-sponsored program, we have begun to provide a firm fundamental understanding of the properties of the Al-containing native oxides of the III-V compound semiconductors, as well as the structural and electrical properties of the chemical interface between the oxide regions and the semiconductor materials.

10.2.1 Studies of Native Oxide Formation

Much of our work on native oxides has focused on the Al-containing III-V ternary alloys InAlP and InAlAs. For comparison, we have also studied the wet oxidation of AlGaAs alloys. Our data indicate that $\text{In}_{0.5}\text{Al}_{0.5}\text{P}$ and $\text{In}_{0.5}\text{Al}_{0.5}\text{As}$ layers oxidize at much slower rate compared to $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$ (note that these ternary compounds all contain the same mole fraction of Al). Also, a higher oxidation temperature ($T_{\text{ox}} \geq 500^\circ\text{C}$) is required to form oxides from $\text{In}_{0.5}\text{Al}_{0.5}\text{P}$ and $\text{In}_{0.5}\text{Al}_{0.5}\text{As}$ compared to $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$ films which oxidize at a substantially lower temperature ($T_{\text{ox}} \sim 450^\circ\text{C}$). Furthermore, the different dependence of the oxide depth upon $(1/T)$ implies a much lower activation energy for $\text{In}_{0.5}\text{Al}_{0.5}\text{P}$ than that of $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$. The reduced activation energy may be a consequence of the presence of "soft" In-P crystal bonds that are more easily broken compared to those of Ga-As or Al-As. The dissociation of these bonds may be a limiting step in the oxidation process³ resulting in lower activation energy for $\text{In}_{0.5}\text{Al}_{0.5}\text{P}$. One of the fundamental issues which we studied in this program is the understanding of the effect of column V elements on the oxidation process and the role of In and Ga column III atoms in the oxidation process.

In another portion of our ARO-sponsored work, we have oxidized the top InAlP cladding layer of an InGaP QW heterostructure sample. The test structure consists of a 200 Å $\text{In}_{0.5}\text{Ga}_{0.5}\text{P}$ QW sandwiched between two 10-period $\text{In}_{0.5}\text{Al}_{0.5}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{P}$ superlattice barriers; where x

varies from 0.5 to 0.45 and each period of the superlattice is $\sim 30\text{\AA}$. The structure has InAlP top (0.25-0.43 μm) and bottom (0.25-0.73 μm) cladding layer and a 450 \AA -GaAs capping layer. For oxidation of the top InAlP cladding of the InAlP/InGaP QW heterostructure, the GaAs cap is selectively removed. After allowing the sample to equilibrate for 5 min before initiating the oxidation process, the exposed InAlP epitaxial layer is longitudinally oxidized for 2-5.5 hours at $\sim 500^\circ\text{C}$ by using H_2O vapor saturated in a N_2 carrier gas (~ 1.0 SLM). Under these conditions, the exposed InAlP is converted to an oxide having an index of refraction of ~ 1.6 with a vertical oxidation rate of $\sim 0.1\text{ }\mu\text{m}/\text{hour}$.

Like SiO_2 , the InAlP native oxide appeared in white light to have different colors depending on the thickness of the oxide. This interference effect, due to the lower index of refraction of the oxide with respect to the underlying InAlP semiconductor, creates a similar color spectrum to that of SiO_2/Si , only with a slight shift of 1.46/1.6 caused by a small difference in the indices of refraction ($n_{\text{SiO}_2} \sim 1.46$ and $n_{\text{Al}_x\text{O}_y} \sim 1.6$).⁴ While we have not confirmed the index by ellipsometry in the present study, the index of refraction of the InAlP native oxide is also approximately 1.6, based on close agreement with the modified color chart. We have also used SEM measurements to more precisely determine the oxide thickness, and thus the oxidation rate. A stained cross-section, obtained by making a fresh cleave and selectively etching the semiconductor epitaxial layers, provided a high level of contrast between the surface oxide layer and the underlying unoxidized InAlP epitaxial layer. SEM micrograph have been made of a $\sim 2200\text{ }\text{\AA}$ oxide that was formed after two hours in $\text{H}_2\text{O} + \text{N}_2$ at 500°C . For the single-layer samples used to measure the oxidation rate, the cleaved specimens were etched in a 50% HCl to provide good etch selectivity for InAlP over the native oxide and the GaAs substrate. For most samples examined, the oxide-semiconductor interface is relatively smooth. A detailed TEM study is required for further investigation of the interface composition and quality. This work is currently on-going.

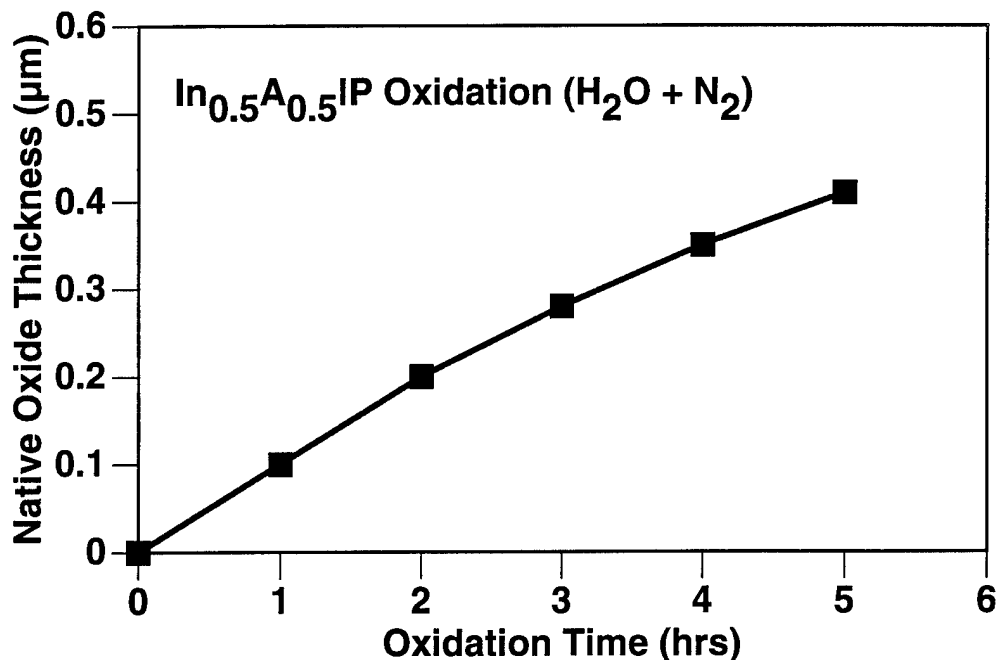


Figure 1: Dependence of oxide thickness upon oxidation time for $\text{In}_{0.5}\text{Al}_{0.5}\text{P}$ alloys.

10.2.2 Photoluminescence Studies of Oxidized QW Heterostructures

In extensive photoluminescence (PL) and time-resolved photoluminescence (TRPL) studies at room temperature we have shown that as a result of the oxidation of the top InAlP cladding, the emission intensity and luminescence lifetime from InGaP SQW increase significantly. Figures 2

and 3 show the room temperature PL spectra for InGaP/InAlP QW heterostructure samples with the top InAlP layer oxidized for various lengths of time. The room-temperature PL peak intensity for the QW heterostructure sample with top InAlP cladding thickness of $0.25\ \mu\text{m}$ increases by a factor of ~ 1.5 when about $0.2\ \mu\text{m}$ of the InAlP is converted to oxide (Figure 2). For the sample with $\sim 0.43\ \mu\text{m}$ top InAlP barrier, the 300 K PL peak intensities are about 1.7 and 3.25 times higher than that from the as-grown sample when $\sim 0.2\ \mu\text{m}$ and $\sim 0.35\ \mu\text{m}$ of the InAlP is oxidized respectively (Figure 3). One of the important goals of our research program is to develop a fundamental understanding of the mechanism through which this improvement occurs.

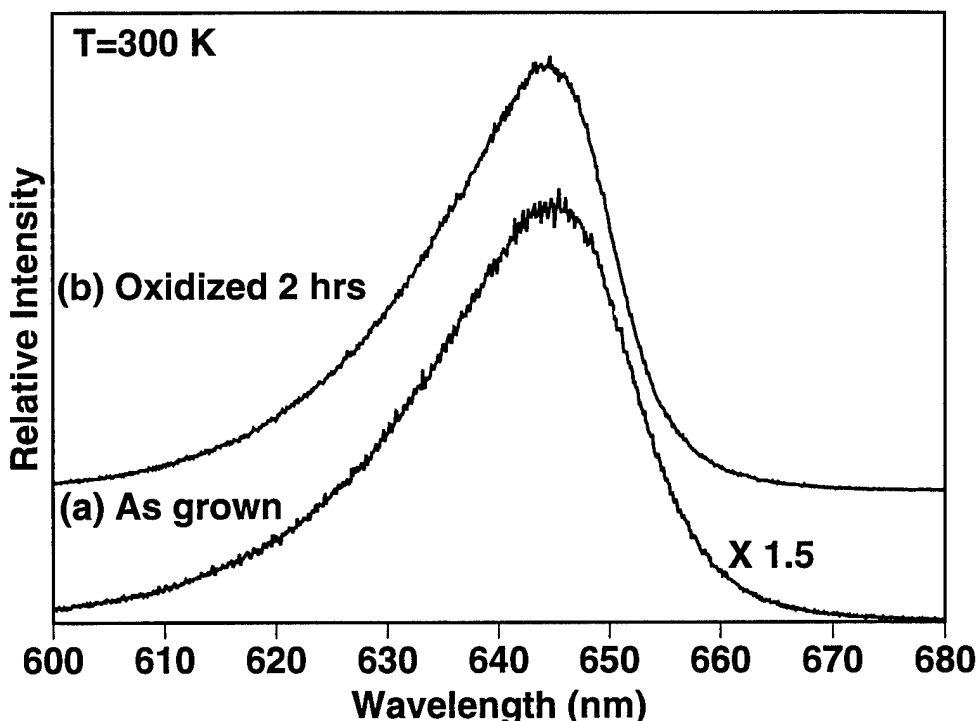


Figure 2: Room temperature PL spectra from an InAlP/InGaP QW heterostructure: (a) an unoxidized sample; (b) a sample from the same wafer that has been oxidized at 500°C for 2 hours.

10.2.3 Time-Resolved Photoluminescence Studies of Oxidized QW Heterostructures

Recently, we have initiated TRPL studies of the luminescence from oxidized and unoxidized InAlP/InGaP QW heterostructures. TRPL experiments at room temperature show that the QW sample with $0.25\ \mu\text{m}$ top InAlP barrier layer has a decay time constant of about 65 ns for all excitation powers when $\sim 0.2\ \mu\text{m}$ of the InAlP is oxidized. (See Figure 4.) The as-grown piece of the same structure exhibits a decay time constant of about 53 ns for all of the excitation intensities measured (ranging over an order of magnitude). The luminescence decay is non-exponential for all of the measurements, displaying characteristics both of high excitation and HSR recombination. These results are, to the best of our knowledge, the first TRPL data taken on III-V compound semiconductor heterostructures containing native-oxide regions. We are in the process of developing a fundamental understanding of the role of the oxidation process on establishing the carrier lifetimes in these structures. It is one of the major goals of the research program to use TRPL to establish the relationship between oxidation and carrier recombination kinetics.

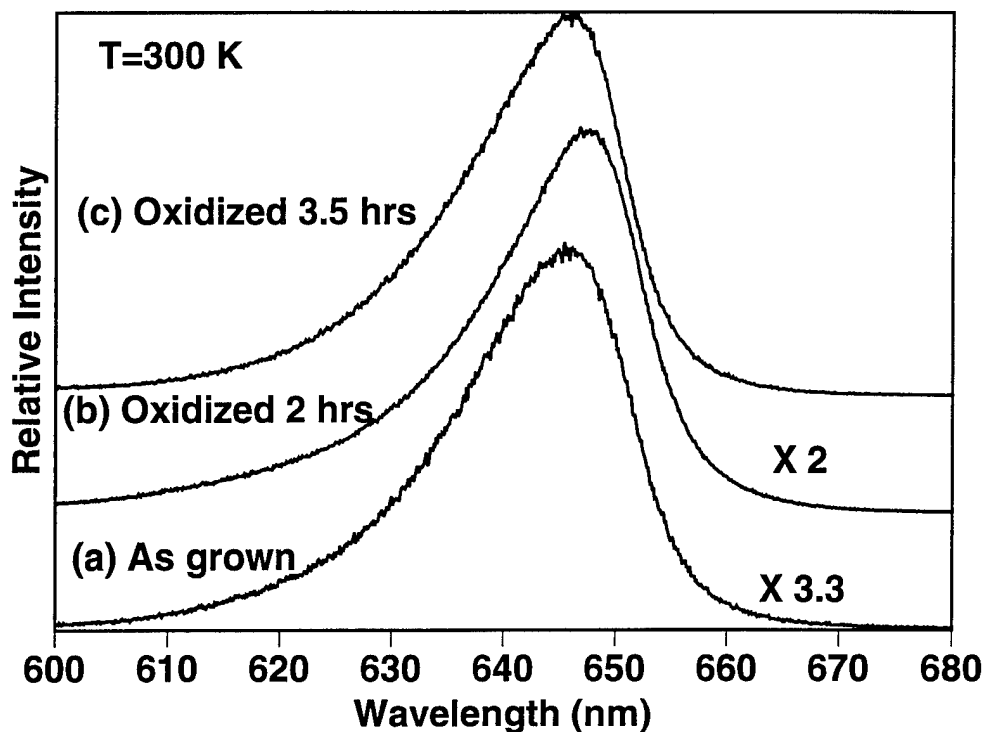


Figure 3: Room temperature PL spectra from an InAlP/InGaP QW heterostructure with InAlP thicker cladding layers: (a) an unoxidized sample; (b) and (c) samples of the same wafer that have been oxidized at 500°C for 2 and 3.5 hours, respectively.

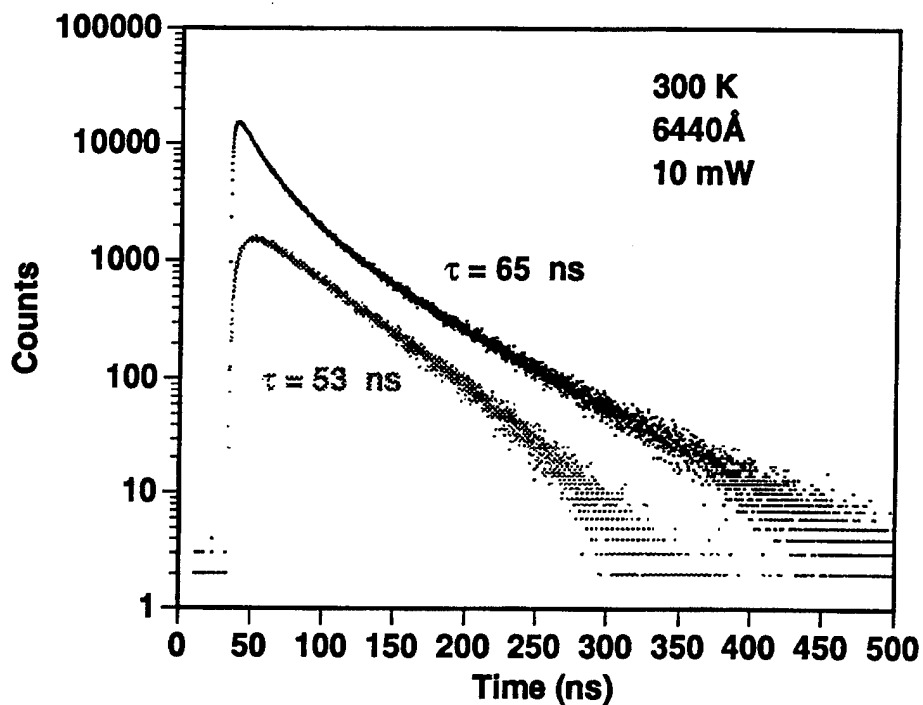


Figure 4: TRPL spectra from as-grown and oxidized InAlP/InGaP QW samples. Note that the luminescence decay time is longer for the oxidized sample.

10.2.4 Secondary Ion Mass Spectrometry Studies

We have already initiated SIMS studies of the native oxides in the InAlGaP system. We have obtained SIMS data for an InAlP/InGaP QW having partially oxidized InAlP top cladding layer formed by wet oxidation of top InAlP at 500°C for different amounts time. These data indicate a chemically sharp interface (within the resolution of the SIMS sputtering) between the oxide and the InAlP. As expected, a significant amount of O and H is present in the oxide. We note that the exact chemical composition of these films cannot presently be determined from these data due to matrix effects and the lack of the necessary standards. In the proposed program we will further explore the effect of oxidation conditions, alloy composition, and doping upon the oxidation rates and the details of the chemical structure of the oxide-semiconductor interface using SIMS.

¹ See Publications #12 and 17

²R. D. Dupuis, M. R. Islam, N. Gardner, and G. E. Stillman, unpublished.

³C. W. Wilmsen, Thin Solid Films **39** 105 (1976).

⁴S. K. Ghandi, *VLSI Fabrication Principles- Silicon and Gallium Arsenide*, (John Wiley and Sons, New York, 1983), pp. 400-414.

Appendix II Publications and Talks Citing Sponsorship of this Contract

Listed below are the refereed publications and talks which cited sponsorship from this contract. Copies of the manuscripts and reprints have been sent with earlier Progress Reports or are included in this Final Technical Report package.

11.1 Publications in Refereed Journals

1. D. L. Huffaker, C. Lei, D. G. Deppe, C. J. Pinzone, J. G. Neff, and R. D. Dupuis, "Controlled Spontaneous Emission in Room-Temperature Semiconductor Microcavities," *Appl. Phys. Lett.*, Vol. 60, pp. 3203-5 (1992).
2. D. L. Huffaker, Z. Huang, C. Lei, D. G. Deppe, C. J. Pinzone, J. G. Neff, and R. D. Dupuis, "Effect on Spontaneous Emission of Quantum Well Placement in a Short Cavity," *Appl. Phys. Lett.*, Vol. 61, pp. 877-9 (1992).
3. Z. Huang, C. Lei, D. G. Deppe, C. C. Lin, C. J. Pinzone, and R. D. Dupuis, "Spectral and Intensity Dependence on Dipole Localization in Fabry-Perot Cavities," *Appl. Phys. Lett.*, Vol. 61, No. 25, pp. 2961-3 (1992).
4. C. Lei, C. J. Pinzone, Z. Huang, D. L. Huffaker, D. G. Deppe, and R. D. Dupuis, "Room Temperature Spontaneous Emission in Five-Micron Long Fabry-Perot Vertical Cavities," *J. Appl. Phys.*, Vol. 73, no. 7, pp. 3153-3157 (1993).
5. C. Lei, Z. Huang, D. G. Deppe, C. J. Pinzone, and R. D. Dupuis, "Spectral and Interference Effects in the Light Emission from Fabry-Perot Cavities," *J. Appl. Phys.*, Vol. 73, no. 6, pp. 2700-2704 (1993).
6. R. D. Dupuis, J. G. Neff, and C. J. Pinzone, "Very Smooth AlGaAs-GaAs Quantum Wells Grown by Metalorganic Chemical Vapor Deposition," *J. Crystal Growth* 124, 558 (1992).
7. R. V. Chelakara, M. R. Islam, J. G. Neff, K. G. Fertitta, A. L. Holmes, F. J. Ciuba, and R. D. Dupuis, "Growth of High-Quality InAlP/InGaP Quantum Wells and InAlP/InGaP Super-Lattice Barrier Cladding Layers by Metalorganic Chemical Vapor Deposition," 7th International Conference on ICMOVPE, Yokohama, Japan, May 1994, published in *J. Crystal Growth*, Vol. 145, pp. 179-186 (1994).
8. J. G. Neff, M. R. Islam, R. V. Chelakara, K. G. Fertitta, F. J. Ciuba, and R. D. Dupuis, "Characterization of GaP/InGaP and GaP/GaAsP Strained-Layer Quantum Wells Grown by MOCVD," 7th International Conference on ICMOVPE, Yokohama, Japan, May 1994, published in *J. Crystal Growth*, Vol. 145, pp. 746-751 (1994).
9. A. L. Holmes, K. G. Fertitta, F. J. Ciuba, and R. D. Dupuis, "X-ray Diffraction Studies of High-Quality GaN Heteroepitaxial Films Grown by Metalorganic Chemical Vapor Deposition," *Elect. Lett.*, Vol. 30, No. 15, pp. 1252-4 (1994).
10. R. V. Chelakara, M. R. Islam, J. G. Neff, K. G. Fertitta, A. L. Holmes, F. J. Ciuba, R. D. Dupuis, T. A. Richard, N. Holonyak, Jr., and K. C. Hsieh, "Short-Wavelength Room-Temperature CW Laser Operation of InAlP-InGaP Superlattices Grown by Metalorganic Chemical Vapor Deposition," *Appl. Phys. Lett.*, Vol. 65, No. 7, pp. 854-7 (1994).
10. K. G. Fertitta, A. L. Holmes, J. G. Neff, F. J. Ciuba, and R. D. Dupuis, "High-Quality GaN Heteroepitaxial Films Grown by Metalorganic Chemical Vapor Deposition," *Appl. Phys. Lett.*, Vol. 65, No. 14, pp. 1823-1825 (1994).
11. C. J. Pinzone, J. G. Neff, R. V. Chelakara, K. Fertitta, and R. D. Dupuis, "The Use of Tetraethyltin as an N Type Dopant Source in GaAs, AlGaAs, and AlAs for Lasers and Bragg Reflectors Grown by MOCVD," Proceedings of the 1994 Fall MRS Meeting, Boston, Massachusetts, November, 1994.
12. T. A. Richard, S. A. Maranowski, N. Holonyak, Jr., E. I. Chen, M. J. Ries, J. G. Neff, P. A. Grudowski, and R. D. Dupuis, "Enhanced Hot-Carrier Spontaneous and Stimulated Recombination in a Photopumped Vertical Cavity $\text{Al}_x\text{Ga}_{1-x}\text{As}$ -GaAs Quantum Well Heterostructure With Multiple Top and Bottom Native Oxide Mirrors," *Appl. Phys. Lett.* Vol. 66, No. 5, pp. 589-591 (1995).

13. T. A. Richard, S. A. Maranowski, N. Holonyak, Jr., E. I. Chen, M. J. Ries; J. G. Neff, P. A. Grudowski, and R. D. Dupuis, "Enhanced Hot-Carrier Spontaneous and Stimulated Recombination in a Photopumped Vertical Cavity $\text{Al}_x\text{Ga}_{1-x}\text{As}$ -GaAs Quantum Well Heterostructure With Multiple Top and Bottom Native Oxide Mirrors," *Appl. Phys. Lett.* Vol. 66, No. 5, pp. 589-591 (1995).
14. R. V. Chelakara, M. R. Islam, and R. D. Dupuis, "Enhancement of Potential Barrier Height by Superlattice Barriers in the InGaAsP/InP Materials System," *Electron. Lett.*, Vol. 31, No. 4, pp. 321-323 (1995).
15. K. G. Fertitta, A. L. Holmes, J. G. Neff, F. J. Ciuba, and R. D. Dupuis and F. A. Ponce, "High-quality GaN Heteroepitaxial Films Grown by Metalorganic Chemical Vapor Deposition," *J. Electron. Mat.*, Vol. 24, No. 4, pp. 257-261 (1995).
16. M. R. Islam, R. V. Chelakara, J. G. Neff, K. G. Fertitta, P. A. Grudowski, A. L. Holmes, F. J. Ciuba, R. D. Dupuis; and J. E. Fouquet, "The Growth and Characterization of AlGaAs Double Heterostructures for the Evaluation of Reactor and Source Quality," *J. Electron. Mat.*, Vol. 24, No. 6, pp. 787-792 (1995).
17. A. L. Holmes, M. R. Islam, C. V. Ramachandran, F. J. Ciuba, R. D. Dupuis, M. J. Ries, N. Holonyak, Jr., "High-Reflectivity Visible-Wavelength Semiconductor Native-Oxide Bragg Reflectors Grown by Metalorganic Chemical Vapor Deposition," *Appl. Phys. Lett.*, Vol. 66, No. 21, pp. 2831-2833 (1995).
18. M. J. Ries, N. Holonyak, Jr., E. I. Chen, S. A. Maranowski, M. R. Islam, A. L. Holmes, and R. D. Dupuis, "Visible-Spectrum ($\lambda = 650$ nm) Photopumped (Pulsed, 300K) Laser Operation of a Vertical-Cavity AlAs-AlGaAs/InAlP-InGaP Quantum Well Heterostructure Utilizing Native Oxide Mirrors," *Appl. Phys. Lett.*, Vol. 67, No. 8, pp. 1107-1109 (1995).
19. M. R. Islam, R. V. Chelakara, R. D. Dupuis, "An InAlP/InGaP Strain-Modulated Aperiodic Superlattice Heterobarrier for Enhanced Electron Confinement in Visible ($\lambda \sim 650$ nm) Light-Emitting Devices," *Appl. Phys. Lett.*, Vol. 67, No. to be published Oct. 2 (1995).
20. M. R. Islam, R. D. Dupuis, and A. L. Holmes, N. F. Gardner, A. P. Curtis, G. E. Stillman, and J. E. Baker, "Enhanced Luminescence From InAlP-InGaP Quantum Wells Having Native-Oxide Windows," *Electron. Lett.*, accepted for publication, to be published 1996.

11.2 Refereed Conference Presentations

1. D. L. Huffaker, D. G. Deppe, C. J. Pinzone, T. J. Rogers, B. G. Streetman, and R. D. Dupuis, "Threshold Dependence on Cavity Length and Mirror Reflectivity in Fabry-Perot Microcavity Semiconductor Lasers with High Contrast Mirrors," presented at IEEE/LEOS Quantum Optoelectronic Topical Meeting, March 17-19, 1993.
2. M. R. Islam, J. G. Neff, R. V. Chelakara, K. G. Fertitta, F. J. Ciuba, and R. D. Dupuis, "MOCVD Growth and Characterization of AlGaP/InGaP/GaP Strained-layer Single Quantum Wells" Presented at the Sixth International Conference on Indium Phosphide and Related Materials, March 27-31, 1994, Santa Barbara CA.
3. R. V. Chelakara, M. R. Islam, J. G. Neff, K. G. Fertitta, A. L. Holmes, F. J. Ciuba, and R. D. Dupuis, "Growth of High-Quality InAlP/InGaP Quantum Wells and InAlP/InGaP Super-Lattice Barrier Cladding Layers by Metalorganic Chemical Vapor Deposition," Presented at The 7th International Conference on ICMOVPE, Yokohama, Japan, May 1994.
4. J. G. Neff, M. R. Islam, R. V. Chelakara, K. G. Fertitta, F. J. Ciuba, and R. D. Dupuis, "Characterization of GaP/InGaP and GaP/GaAsP Strained-Layer Quantum Wells Grown by MOCVD," Presented at The 7th International Conference on ICMOVPE, Yokohama, Japan, May 1994.
5. C. J. Pinzone, J. G. Neff, R. V. Chelakara, K. Fertitta, and R. D. Dupuis, "The Use of Tetraethyltin as an N Type Dopant Source in GaAs, AlGaAs, and AlAs for Lasers and Bragg Reflectors Grown by MOCVD," Presented at the 1994 Fall MRS Meeting, Boston, Massachusetts, November, 1994.

6. R. V. Chelakara, M. R. Islam, J. G. Neff, K. G. Fertitta, P. A. Grudowski, A. L. Holmes, F. J. Ciuba, and R. D. Dupuis, "The Growth and Characterization of AlGaAs Double Heterostructures for the Evaluation of Reactor and Source Quality," International Symposium on Compound Semiconductors, San Diego, 18-22 September 1994.
7. (Invited) R. D. Dupuis, "High-Quality AlGaN Heteroeptiaxial Films Grown by Metalorganic Chemical Vapor Deposition," Northern California Materials Research Conference, San Jose, CA, 20-21 March 1995.
8. F. A. Ponce, K. G. Fertitta, A. L. Holmes, J. G. Neff, F. J. Ciuba, and R. D. Dupuis, "Crystalline Structure of GaN Epitaxy on Sapphire Using GaN Buffer Layers," 1995 Spring Meeting of the Materials Research Society, San Francisco CA, April 1995.
9. M. R. Islam, R. V. Chelakara, J. G. Neff, and R. D. Dupuis, "Growth and Characterization of InAlP-InGaP Modulated-Strain Superlattice-Barrier Quantum-Well Heterostructures," 1995 Electronic Materials Conference, Charlottesville VA, 21-23 June 1995.
10. A. L. Holmes, and R. D. Dupuis, "Growth and Characterization of InAlP-InGaP Modulated-Strain Superlattice-Barrier Quantum-Well Heterostructures," 1995 Electronic Materials Conference, Charlottesville VA, 21-23 June 1995.
11. (Invited) R. D. Dupuis and F. A. Ponce, "High-Quality III-V Nitrides Grown by Metalorganic Chemical Vapor Deposition," Paper We-1010, Fifth International Conference on the Formation of Semiconductor Interfaces, Princeton, NJ, 26-30 June 1995.
12. (Invited) R. D. Dupuis and F. A. Ponce, "High-Quality AlGaN Heteroeptiaxial Films Grown by Metalorganic Chemical Vapor Deposition," National Science Foundation Forum on Optical Science and Engineering, SPIE Meeting July 11-12, 1995. SPIE Proceedings.
13. M. R. Islam, R. V. Chelakara, R. Dupuis, N. Gardner and G. E. Stillman, "Improvement of Luminescence Properties of InGaP/InAlP QW Heterostructures with Oxidized InAlP Cladding Layers Grown by MOCVD" Paper OMP 4.4 presented at the 1995 IEEE/LEOS Annual Meeting, October 30-November 2, 1995, San Francisco CA.

11.3 Theses Completed Under This Program

Master's Theses: None

Ph.D. Theses:

Chun Lei: "Spontaneous Emission in Semiconductor Microcavities and It's Role in Vertical Cavity Surface Emitting Lasers," May 1993.

Abraham Shen Tong, "The Monolithic Integration of Indium Alloy Heterojunction Bipolar Transistors and Light Emitting Diodes," December 1995.

Ramachandran V. Chelakara, "MOCVD Growth of InGaAs/InAlAs/InP and InGaP/InAlP/GaAs Based Heterostructures for HBT's and Light Emitting Devices," May 1996.

Appendix III Technical Personnel Participating In This Program

12.0 Participating Technical Personnel Sponsored During Program

Professors:

Dr. Russell D. Dupuis, Dr. Christine Maziar, Dr. Dennis G. Deppe

Graduate Students:

Mr. Ramachandran V. Chelakara, Dr. Abraham S. Tong, Dr. Chun Lei, Vishnu Bhat.